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MOTion Trap Experiment – Control Unit

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1. Rationale

The MOTion trap experiment incorporates a combined linear radio-frequency (RF) trap with a time-of-flight (TOF) mass spectrometer (MS). Once trapped, the ions can be cooled and manipulated and, subsequently, kicked out *radially* into the TOF MS. The ions-of-choice are Yb^+ and $Ba^+/BaCl^+$.

The RF trap consists of four rods which are all segmented into three segments. The trap has a field radius $R_0 = 6.85\,\mathrm{mm}$, a rod diameter of $r = 9.02\,\mathrm{mm}$ and a distance $Z_0 = 10.67\,\mathrm{mm}$ from the center of the trap to an outer segment. The RF trap is operated asymmetrically, i.e.two opposing rods are driven by an RF voltage and the other two rods are at RF ground (GND). We aim for a Mathieu parameter $q < 0.2$ and choose an RF drive frequency of $\Omega = 2\pi \times 1.8\,\mathrm{MHz}$ for normal trap operation and $\Omega_{\mathrm{alt}} = 700\,\mathrm{kHz}$ as alternative RF drive frequency. The maximum RF voltage is $V_{\mathrm{RF}} = 750\,\mathrm{V}$. Additionally, each segment allows for adding an independent (positive) DC voltage $U_n \leq 15\,\mathrm{V}$ to provide the axial confinement of the ions, an optional Mathieu a parameter, and micromotion/stray field compensation.

For the TOF operation, the RF drive voltage is turned off within half a cycle of Ω. Afterwards, DC high voltages (HVs) of up to 1.5 kV are applied to each segment of the RF trap with a rise time of $T_{\mathrm{HV}} \sim 250\,\mathrm{ns}$ (10 % to 90 %). Here, the rods closest to the TOF MS have a slightly lower voltage $HV^{<}$ than the far rods with $HV^{>}$.

We choose a design with an individual drive electronics for each of the 12 segments of the RF trap. Thus, we have a fine-grained control over the individual RF/DC voltages and HVs. These 12 drive electronics (see Sec. **??** are controlled from a control unit (see Sec. 2) that provides 16 synchronized RF sources plus trigger and timing circuitry for RF shut-down and activation of the HV pulses. The control unit is configured by a PC using a serial communication over USB.

2. Control Unit

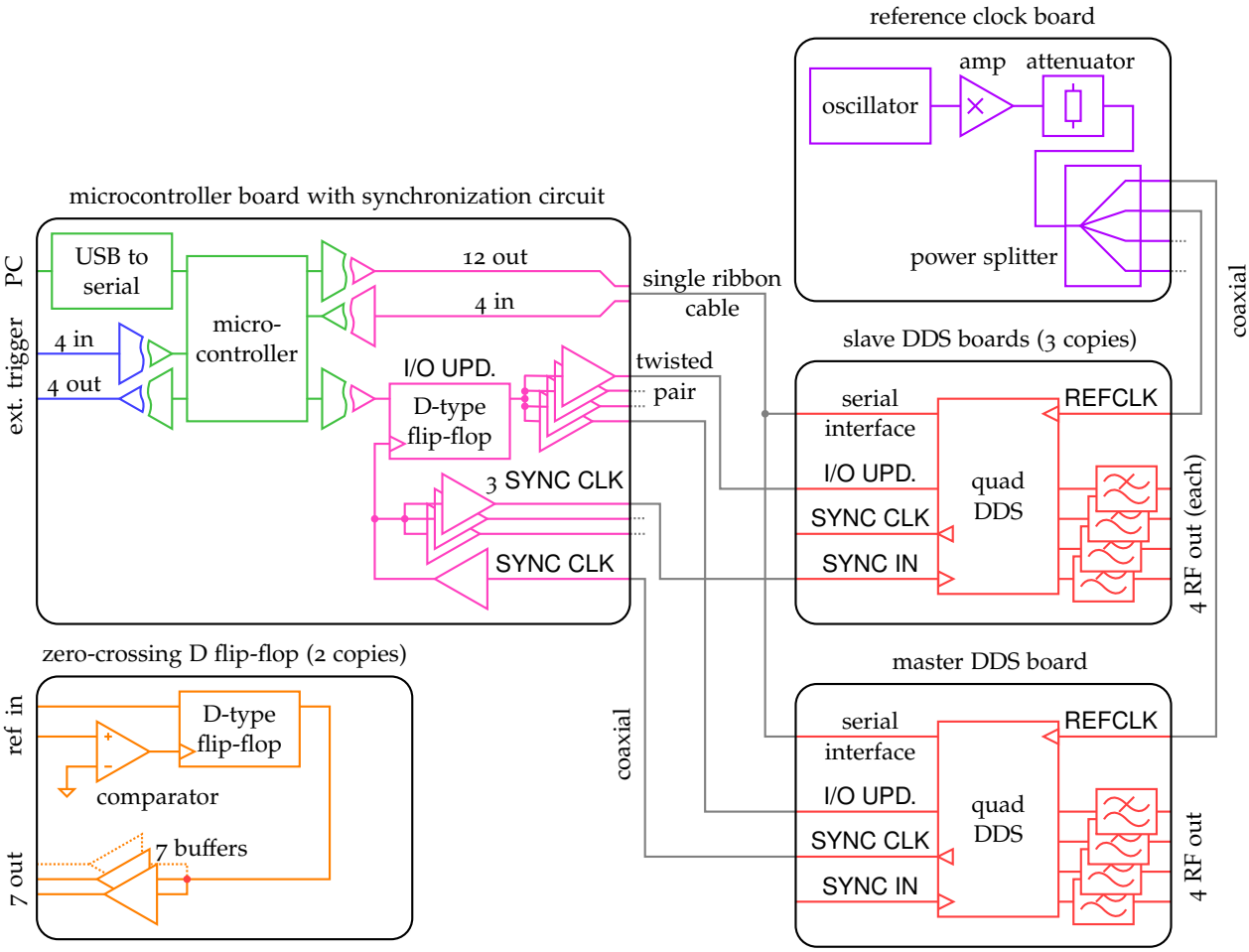


Figure 1: Block diagram of the control unit. See text for explanation.

The control unit (see Fig. 1 for a schematic overview) consists of multiple printed-circuit boards:

- four Analog Devices AD9959 quad-DDS evaluation boards providing in total 16 RF outputs (Sec. 2.1),
- a microcontroller board with synchronization ciruitry; it allows to program the DDS boards from a PC via a serial communication and perform real-

time tasks such as turning off all RF outputs upon external trigger signals (Sec. 2.2),
- a 500 MHz clock source with four outputs, one for each DDS board (Sec. 2.3),
- two zero-crossing D-type flip-flop boards; these boards make it possible to generate from an (unsynchronized) input TTL signal (seven buffered) output TTL signals whose rising edge is aligned with the zero-crossing of a reference RF signal (Sec. 2.4),
- and a power supply providing various supply voltages (1.8 V, 3.3 V, and 5.0 V) for the different parts of the boards (not shown in Fig. 1).

The individual components will be described in more detail in the following.

2.1. DDS Boards

For general information about the DDS evaluation boards (AD9959/PCBZ) and the DDS chip itself (AD9959) the reader is referred to the datasheets on the Analog Devices Website. A brief description follows below.

2.1.1. Description

For the generation of the RF we choose Analog Devices AD9959 evaluation boards, which feature four DDS channels each with individual frequency, phase, and amplitude control.

Basically, each DDS core has a 32-bit phase accumulator, which is incremented by the frequency tuning word (FTW) during each cycle of the system clock (SYSCLK). The value of the phase accumulator $\in [0, 2^{32} - 1]$ corresponds to the phase of the output cosine wave $\in [0, 2\pi)$. A phase-to-amplitude converter translates the phase value to an amplitude, which is output with a 10-bit digital-to-analog converter (DAC). Hence, the output frequency is

$$f_{\text{out}} = \frac{f_{\text{SYSCLK}} \times \text{FTW}}{2^{32}}.$$

Additionally, each core allows to add a constant phase offset (phase offset word (POW), 14 bits) and scale the output amplitude (amplitude scale factor, 10 bits).

The boards are configured via an Serial Peripheral Interface (SPI) interface (the onboard USB interface is not being used). The reader is referred to the datasheet for a more detailled description of all the features.

2.1.2. Synchronization

All four DDS evaluation boards are synchronized. The basics for understanding the requirements for the synchronization and its implementation in the control unit are briefly discussed below. The reader is referred to the datasheets of the AD9959 for details on the used synchronization mode (automatic mode synchronization).

Each DDS board derives various internal clock signals from the externally provided reference clock (REFCLK). For successful synchronization of all four DDS boards, the REFCLK signals for all boards should have as little mutual phase difference as possible. This is achieved with the clock source (see Sec. 2.3) and the use of SMA cables of equal length (12 in) to connect each DDS board to the clock source.

The SYSCLK is derived from the REFCLK by multiplying it with a software-configurable phase-locked loop (PLL) divider ratio (M). A higher REFCLK frequency provides better phase-noise characteristics. We use the maximal REFCLK frequency of 500 MHz, which requires a PPL divider ratio of $M = 1$, such that REFCLK and SYSCLK rates are identical.

The synchronization clock (SYNC_CLK) runs at one-forth of the SYSCLK and determines the speed of the serial interface. Upon reset, the DDS boards have random mutual SYNC_CLK phase differences of about 0 °, 90 °, 180 °, or 270 °. To synchronize them, the SYNC_CLK of a master DDS board is connected to the SYNC_IN of the slave boards. Master/slave and the synchronization mode are configured in software via the serial interface.

Connecting the SYNC_CLK output of the master board directly to the slave boards deteriorated the signal too much and required individual buffering, which is part of the synchronization circuit on the microcontroller board (see red parts in Fig. 1 and Sec. 2.2). The buffer outputs are connected to the slave DDS boards with SMA cables of identical length (12 in).

Finally, a potential (now deterministic!) phase difference between the master and slave boards due to a signal propagation delay of the SYNC_CLK can be adjusted in software.[1]

Lastly, the I/O_UPDATE transfers data from the serial I/O buffer of a DDS chip to the active registers of the DDS cores. All four DDS boards must receive coincident I/O_UPDATE rising edges for being synchronized. Otherwise, one DDS board might run one or more SYSCLK cycles earlier at a different frequency than the other DDS boards leading to a phase difference of the output RF signals.

[1] It turned out to be zero in our box.

The clock of the microcontroller and, thus, its digital signals are not phase-locked to the SYNC_CLK of the DDS boards. Even coincident I/O_UPDATEs from the microcontroller can destroy the synchronization, because small phase differences between the SYNC_CLKs can with a small probability result in some DDS boards to update the active registers one SYSCLK cycle before the others. As a solution, the I/O_UPDATE signal from the microcontroller is passed through an edge-triggered D-type flip-flop, which transfers the signal to its output upon the rising edge of the master's SYNC_CLK (see red parts in Fig. 1 and Sec. 2.2).

There is an individual buffer for the I/O_UPDATE for each DDS board to ensure a good signal quality and again cables with same length (twisted-pair cables, preferably short) are used to connect each board.

The length of the SMA cable from the master's SYNC_CLK output to the microcontroller board can be used to shift the rising edges of the I/O_UPDATE and SYNC_CLK sufficiently apart.[2]

[2] A 12 in SMA cable did the trick by chance. The length required for a shift of 180° would be about 80 cm.

2.2. Microcontroller Board

2.2.1. Description

The microcontroller board is based on an Atmel ATmega2560 microcontroller with an FTDI FT232RL USB-to-serial converter (see green parts in Fig. 1 and sheets 1 and 2 of the schematics). The USB-to-serial converter and the microcontroller itself are powered via USB from the connected PC (resulting in 5 V logic levels). The microcontroller is largely compatible with the Arduino Mega2560 board. For example, the Arduino bootloader has been programmed to the microcontroller such that the main firmware can now be flashed over the USB port (just as with the Arduino board) instead of flashing it using Atmel's in-system programmer (ISP) interface.

Expect for the USB connection, all the other digital connections from/to the microcontroller are lead through digital isolators and are powered from the power supply of the control unit. Hence, both the digital inputs/outputs and the RF outputs of the control unit are galvanically decoupled from the PC protecting it and preventing ground loops. In addition, the isolators buffer the inputs/outputs of the microcontroller and interface 5 V and 3.3 V logic.

2.2.2. Serial Interface for the DDS

Connector X7 of the microcontroller board provides the serial interface to the DDS boards. It has 4 inputs and 12 outputs with 3.3 V logic levels (see red parts in Fig. 1 and sheet 4 of the schematics). It contains all the non-timing-critical signals and is optimized for the single-bit 3-wire SPI mode of the AD9959 (see datasheet for details): Registers are written to the DDS chip over a serial-data-in (SDI) wire and read over a serial-data-out (SDO) wire with a common serial clock (SCLK) wire.

All DDS chips share (= are connected in parallel to) reset (RESET), serial clock (SCLK), serial data in (SDI), sync I/O (SYNC_I/O), and profile pins (P0 to P3 enabling fast switching between certain register values). However, separate outputs for the chip select ($\overline{\text{CS}}$) and separate inputs for the serial data out (SDO) of each DDS chip are provided (see Tab. 1 for the pin mappings).

To facilitate the wiring, passive DDS chain boards adapt connectors U2 and U13 of the AD9959 DDS evaluation boards to a single ribbon cable connector with the same pin assignments as X7 on the microcontroller board (see Tab. 1). These DDS chain boards also provide configuration options to connect the proper SDO_x and $\overline{\text{CS}}_x$ of X7 to the SDO and $\overline{\text{CS}}$ of the x-th DDS board, respectively. A single ribbon

cable interconnects the serial interfaces of the microcontroller and all DDS chain boards.

Optionally, if the DDS boards do not require synchronization, connector X7 can also provide a shared I/O_UPDATE. The DDS chain boards can be configured to use this I/O_UPDATE, not requiring to wire up the individually buffered, synchronized I/O_UPDATEs from connector X2 to each DDS chain board.

2.2.3. Synchronization Circuit for the DDS

For the details on how the synchronization of the DDS boards works see also Sec. 2.1.2 and the datasheet of the AD9959. The circuit can be found on sheet 3 of the schematics.

Initially, two options for synchronizing I/O_UPDATE with the SYNC_CLK of the DDS chips were considered:

A. using a quartz oscillator as clock for the microcontroller and syncronizing I/O_UPDATE with an edge-triggered D-type flip-flop, which is sketched in Fig. 1 and described in Sec. 2.1.2, or
B. dividing the SYNC_CLK from the DDS by eight and using it as clock for the microcontroller, such that any microcontroller signal is automatically phase-aligned with the SYNC_CLK.

Option A works and is used in the control unit. Option B does not work, because resetting the DDS boards turns off their SYNC_CLK pin and, thus, the clock for the microcontroller, which stalls the system. Still, option B might be useful in a different scenario with a different, where the external clock is not derived from the DDS board. See Tab. 6 for the jumper settings of the microcontroller board.

The cables from the SYNC_CLK_OUT connectors to the slave DDS boards' SYNC_IN connectors must have the same length (12 in). The length of the cable from the master's SYNC_CLK to the SYNC_CLK_IN of the microcontroller board can be used to tune the phase difference between SYNC_CLKs and I/O_UPDATEs. Here, a 12 in cable turned out to be fine.

Caveat: Note that the master's SYNC_CLK has to be used on connector X3, *not* the SYNC_OUT signal. The clock signal must be available right after turn-on of the box to be able to generate I/O_UPDATE signals via the edge-triggered D-type flip-flop for software-configuring the DDS chips. The SYNC_CLK is available upon turn-on, while the SYNC_OUT will only be available *after* configuring the corresponding board as the master board (which will not be possible, because there will be no I/O_UPDATE).

Connector X2 is described in Tab. 3. The I/O_UPDATE signals must be connected to the DDS boards (more precisely, the chain boards) with twisted-pair cables (one I/O_UPDATE and one GND1 per pair) of identical lengths.

2.2.4. External Digital I/O

The external digital I/O connector X9 is accessible from the front of the box and provides 4 interrupt capable inputs and 4 outputs (5 V TTL levels; blue parts in Fig. 1). Two of the interrupts are edge-triggered (INTx) and two are triggered upon (any) pin change (PCINTx).

Caveat 1: Each input/output has a resistor in series, to prevent damage from (small) voltages applied to outputs or (slight) over-voltages applied to inputs. If the externally connected device has an input with comparatively low input impedance (smaller than several kΩ), the outputs on connector X9 might not be able to reach the logic-high level.

Caveat 2: (Only for older microcontroller board revisions before "rev20150217".) If input pins are not used, they must be (externally) connected to ground, e.g. with pull-down resistors or shorts. Otherwise, the high impedance of the input pins can lead to spurious trigger events on unconnected pins, if a close-by pin experiences a level change.

To work around caveat 2 and for easy-of-use, an extra PCB has been made, which adapts the signals on X9 to SMA connectors and provides pull-down resistors for the 4 inputs (see Sec. A.3).

The pin mappings are given in Tab. 4.

2.2.5. Optional Digital Interface

The microcontroller board provides an additional, currently unused, digital interface with 8 inputs and 8 outputs (not shown in Fig. 1). It provides 3.3 V logic levels by default, which can be changed by substituting IC19 with a 5 V regulator. For completeness, the pin mappings are given in Tab. 5.

2.2.6. Jumper Settings

The jumper settings for the microcontroller board are given in Tab. 6.

ATmega2560	schematics	pin of X7	AD9959	software
–	VCC1	1	–	–
–	VCC1	2	–	–
PD7	DI3	5	SDO_3	SDO3
PD6	DI2	7	SDO_2	SDO2
PD5	DI1	9	SDO_1	SDO1
PD4	DI0	11	SDO_0	SDO0
PD3	DO11	13	SYNC_I/O	SYNCIO
PD2	DO10	15	RESET	RESET
PD1	DO9	17	SCLK	SCLK
PD0	DO8	19	SDI	SDI
PL7	DO7	21	$\overline{CS}_3$	NCS3
PL6	DO6	23	$\overline{CS}_2$	NCS2
PL5	DO5	25	$\overline{CS}_1$	NCS1
PL4	DO4	27	$\overline{CS}_0$	NCS0
PL3	DO3	29	P3	P3
PL2	DO2	31	P2	P2
PL1	DO1	33	P1	P1
PL0	DO0	35	P0	P0
PG3	IOUPDATE	37 (optional!)	I/O_UPDATE	IOUPDATE

Table 1: Pin mappings for microcontroller ATmega2560 (IC2) pins to signal names in schematics, to pins of ribbon cable connector (X7), to pins of DDS chip AD9959, to macro names in the software (see Sec. **??**). The indeces of SDO and $\overline{CS}$, respectively, in the column labelled AD9959 denotes the DDS board number it will be connected to. Signals DI*x* denote input signals of the ATmega2560, while DO*x* denote outputs. Note that I/O_UPDATE on pin 37 of X7 is optional (pin is ground by default!) and only useful, if the DDS boards do not require synchronization. All other pins of connector X7 not mentioned above are held at ground GND1.

connector	signal	connected to
X3	SYNC_CLK_IN	SYNC_CLK of master DDS board
X4	SYNC_CLK_OUT	SYNC_IN of first slave DDS board
X5	SYNC_CLK_OUT	SYNC_IN of second slave DDS board
X6	SYNC_CLK_OUT	SYNC_IN of third slave DDS board

Table 2: SYNC_CLK input and outputs.

pin	signal
1	VCC1
3	I/O_UPDATE
5	I/O_UPDATE
7	I/O_UPDATE
9	I/O_UPDATE

Table 3: Pin mappings of connector X2. All other pins are ground GND1.

ATmega2560	schematics	pin of X9	special function
–	VCC3	1	–
PE5	XI3	3	INT5
PE4	XI2	5	INT4
PK0	XI0	7	PCINT16
PK1	XI1	9	PCINT17
PK4	XO0	11	–
PK5	XO1	13	–
PK6	XO2	15	–
PK7	XO3	17	–

Table 4: Pin mappings for microcontroller ATmega2560 (IC2) pins to signal names in schematics, to pins of ribbon cable connector (X9), and special function for interrupt capable pins (see Sec. **??**). Signals XI*x* denote input signals of the ATmega2560, while XO*x* denote outputs. All other pins of connector X9 not mentioned above are held at ground GND3.

ATmega2560	schematics	pin of X8
–	VCC2	1
–	VCC2	2
PJ7	AO7	5
PJ6	AO6	7
PJ5	AO5	9
PJ4	AO4	11
PJ3	AO3	13
PJ2	AO2	15
PJ1	AO1	17
PJ0	AO0	19
PC7	AI7	21
PC6	AI6	23
PC5	AI5	25
PC4	AI4	27
PC3	AI3	29
PC2	AI2	31
PC1	AI1	33
PC0	AI0	35

Table 5: Pin mappings for microcontroller ATmega2560 (IC2) pins to signal names in schematics, to pins of ribbon cable connector (X8). Signals AI*x* denote input signals of the ATmega2560, while AO*x* denote outputs. All other pins of connector X8 not mentioned above are held at ground GND2.

jumper	description
JP1	closed (default): microcontroller reset upon initialization of USB-to-serial interface open: otherwise
JP2	1-2 and 3-4 closed, 5-6 open (default): quartz oscillator used as clock of microcontroller 1-2 and 3-4 open, 5-6 closed: external clock used for microcontroller
JP3	Atmel ISP interface for (initially) flashing the bootloader to the microcontroller and changing the so-called fuse settings; do not add any jumpers!
JP4	1-2 open, 3-4 closed (default): I/O_UPDATE is synchronized by D-type flip-flop 1-2 closed, 3-4 open: I/O_UPDATE is either unsynchronized or the clock of the microcontroller must be synchronized to SYNC_CLK
JP5	1-2 open, 3-4 closed (default): SYNC_CLK passed to D-type flip-flop for synchronization 1-2 closed, 3-4 open: SYNC_CLK passed to clock divider IC7; see its datasheet for setting the appropriate clock divider ration using solder jumpers SJ1 and SJ2
JP6	1-2 open, 3-4 closed (default): connector X7 does not provide an I/O_UPDATE signal 1-2 closed, 3-4 open: connector X7 provides I/O_UPDATE (see Tab. 1); use only for unsynchronized DDS boards!
JP7	closed (default): provide power of DDS serial interface and syncronization circuit from microcontroller board; VCC1 pins of connector X7 provide that voltage for externally connected devices open: sub-circuit powered down or powered (externally) from VCC1 pins of connector X7
JP8	closed (default): provide power of optional digital interface from microcontroller board; VCC2 pins of connector X8 provide that voltage for externally connected devices open: sub-circuit powered down or powered (externally) from VCC2 pins of connector X8
JP9	closed (default): provide power of external digital interface from microcontroller board; VCC3 pins of connector X9 provide that voltage for externally connected devices open: sub-circuit powered down or powered (externally) from VCC3 pin of connector X9

Table 6: Jumper settings of the microcontroller board.

2.3. Reference Clock Board

2.3.1. Description

The reference clock board provides 4 REFCLK signals (500 MHz, ≈ 8 dBm each) with *same phase*—one for each of the 4 DDS boards (see Fig. 1). The REFCLKs are to be connected to the DDS boards with cables of identical length (12 in were chosen here). The components are listed in Tab. 7.

oscillator	Crystek RFPRO33-500.00
amplifier	Mini-Circuits ZX60-33LN-S+
attenuator	Mini-Circuits VAT-*x*+
power splitter	Mini-Circuits ZB4PD1-500+

Table 7: Components of the reference clock board.

The attenuation value has been chosen such that the power of the REFCLK signals has the desired value. It must be adapted, if any of the RF components is replaced (even with same model) or substituted by another model.

2.4. Zero-Crossing D-Type Flip-Flop Boards

2.4.1. Description

These boards pass changes of an input TTL signal TTL_IN to 7 buffered outputs TTL_OUT upon zero-crossing (from negative to positive) of an analog RF reference signal REF (see Fig. 1, orange circuit). REF is (by default) an RF input with 50 Ω impedance and TTL_IN (TTL_OUT) are 5 V TTL inputs (outputs).

The boards are used to generate trigger signals for the HV pulsing which are phase-stable with respect to the RF voltage. This is important, because the performance of the damping of the trap RF voltage and the shape of the subsequent HV pulses depends strongly on the RF phase at which it has been initiated.

Two DDS channels running at the currently used RF drive frequency are used as references $\mathrm{REF}_{1/2}$ for both flip-flop boards. One of the flip-flop boards receives an external, uncorrelated trigger signal for the HV pulsing. Its outputs are used to trigger the HV pulsing of the drive boards tuned to 1.8 MHz resonant frequency *and* the second flip-flop board. The other flip-flop board then triggers the drive boards tuned to 0.7 MHz resonant frequency. By changing the phase $\varphi_{1/2}$ between $\mathrm{REF}_{1/2}$ and the DDS channels used for the RF drive electronics, the timing of the RF pulsing can be optimized.

Note: The input trigger for the second flip-flop board must be provided by the first flip-flop board. If the same (uncorrelated) external trigger was used by both flip-flop boards, the flip-flop board with reference dragging behind ($\varphi_x > \varphi_y$) would sometimes be triggered one RF drive period before the other flip-flop board and the HV pulses would not coincide.

Caveat: There is still a small window around a certain phase difference $\varphi_1 - \varphi_2$, at which TTL_OUT from the first flip-flop board is detected by the second flip-flop board at about the same time as the zero-crossing of REF_2 occurs. In that case, there will still be sometimes jumps (by one period of the drive RF) of the HV pulses of the 0.7 MHz boards. As a solution, the trigger delay of the 0.7 MHz drive boards can be changed or slightly different phases $\varphi_{1/2}$ be used.

Caveat: The jitter in the detection of the zero-crossing of the REF signals increases with decreasing amplitude of the REF signal. In addition, due a small hysteresis voltages in detecting the zero-crossing, TTL_OUT will be slightly shifted for decreasing amplitudes of REF. For lowest jitter (typically < 5 ns for our RF frequencies) and shift, it is strongly recommended to operate the REF DDS channels at their maximal amplitude ($\sim 350\,\mathrm{V_{pp}}$). (The maximal amplitude for REF should not exceed $5\,\mathrm{V_{pp}}$.)

2.4.2. Jumper Settings

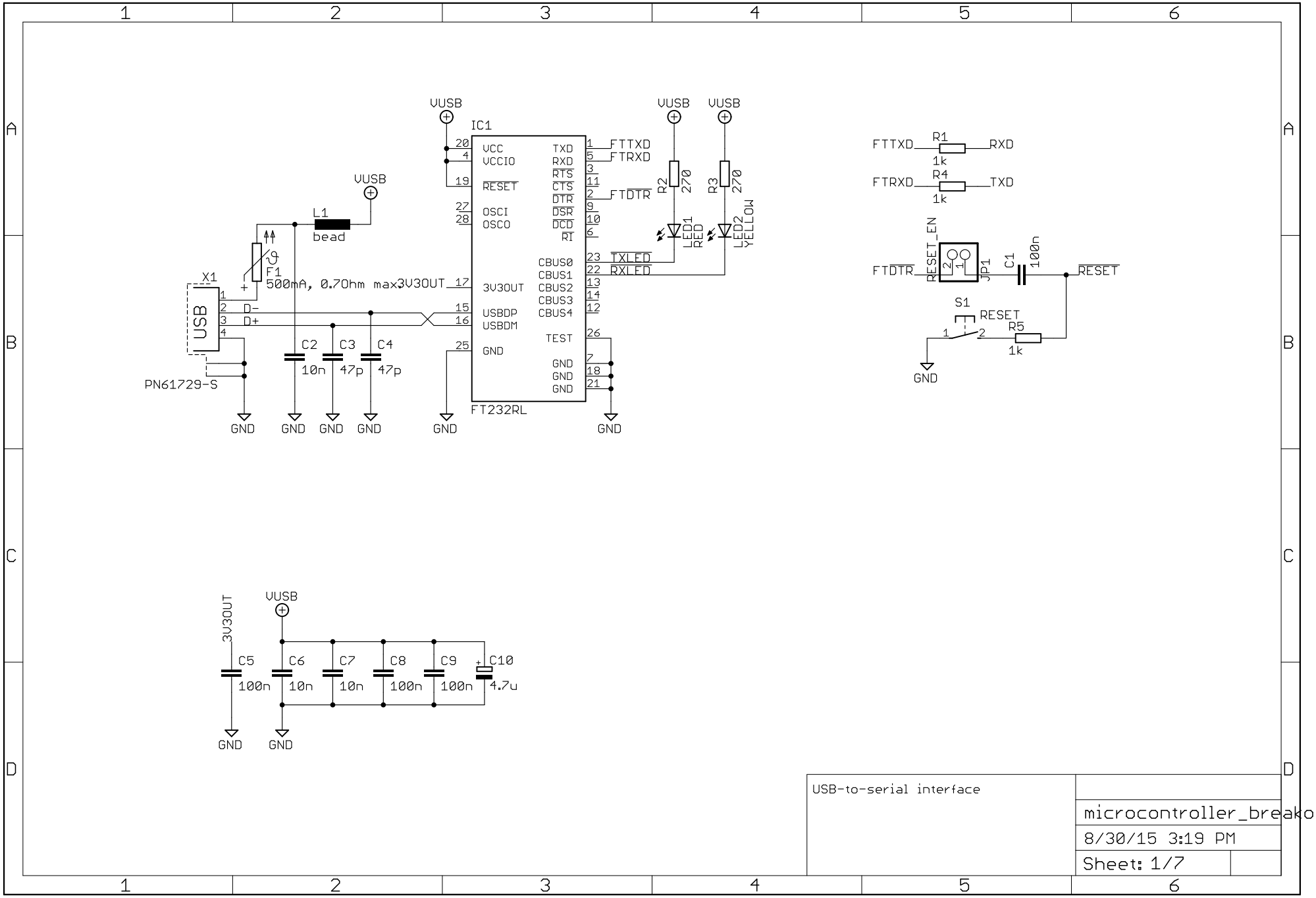
The jumper settings for the zero-crossing D-type flip-flop boards are given in Tab. 8.

jumper	description
JP1	closed (default): power enabled open: powered down
JP2	internal connector for TTL_IN (actually not a jumper)
JP3	internal connector for TTL_OUT (actually not a jumper)
JP4	1-2 open, 3-4 closed (default): TTL_OUT is synchronized by D-type flip-flop to zero-crossing of REF 1-2 closed, 3-4 open: TTL_OUT is not synchronized to REF (= simple buffering of TTL_IN)
JP5/JP6	1-2 closed (default): REF input is a 50 Ω analog RF input; synchronization to zero-crossing 2-3 closed: REF is a 5 V TTL input; synchronization to rising edge *Important:* JP5 and JP6 must have the same configuration!

Table 8: Jumper settings of the zero-crossing D-type flip-flop board.

A. Schematics and PCB Layouts

A.1. Microcontroller Board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IC1
VCC
VCCIO
RESET
OSCI
OSCO
3V3OUT
USBDP
USBDM
GND
TXD
RXD
RTS
CTS
DTR
DSR
DCD
RI
CBUS0
CBUS1
CBUS2
CBUS3
CBUS4
TEST
FTTXD
FTRXD
FTDTR
TXLED
RXLED
R2 270
R3 270
LED1 RED
LED2 YELLOW
L1 bead
F1 500mA, 0.7Ohm max
X1 USB
D-
D+
PN61729-S
C2 10n
C3 47p
C4 47p
FT232RL
R1 1k
R4 1k
RESET_EN
JP1
C1 100n
RESET
S1
R5 1k
3V3OUT
C5 100n
C6 10n
C7 10n
C8 100n
C9 100n
C10 4.7u
GND
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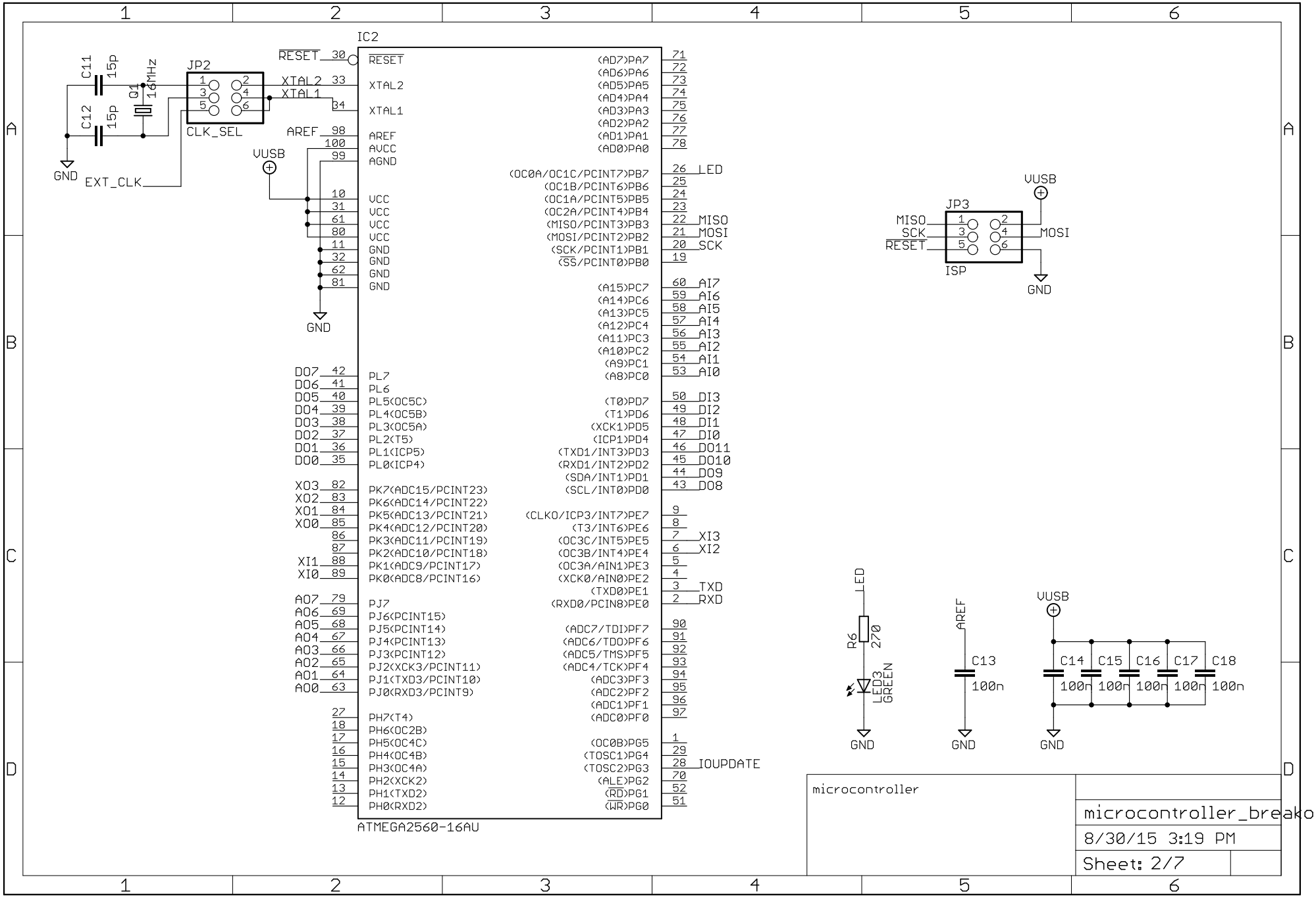
Sheet: 1/7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JP2
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C11 15p
C12 15p
Q1 16MHz
GND
EXT_CLK
RESET 30
XTAL2 33
XTAL1 34
AREF 98
AVCC 100
AGND 99
VUSB
VCC 10 31 61 80
GND 11 32 62 81
D07 42
D06 41
D05 40
D04 39
D03 38
D02 37
D01 36
D00 35
XO3 82
XO2 83
XO1 84
XO0 85
86
87
XI1 88
XI0 89
AO7 79
AO6 69
AO5 68
AO4 67
AO3 66
AO2 65
AO1 64
AO0 63
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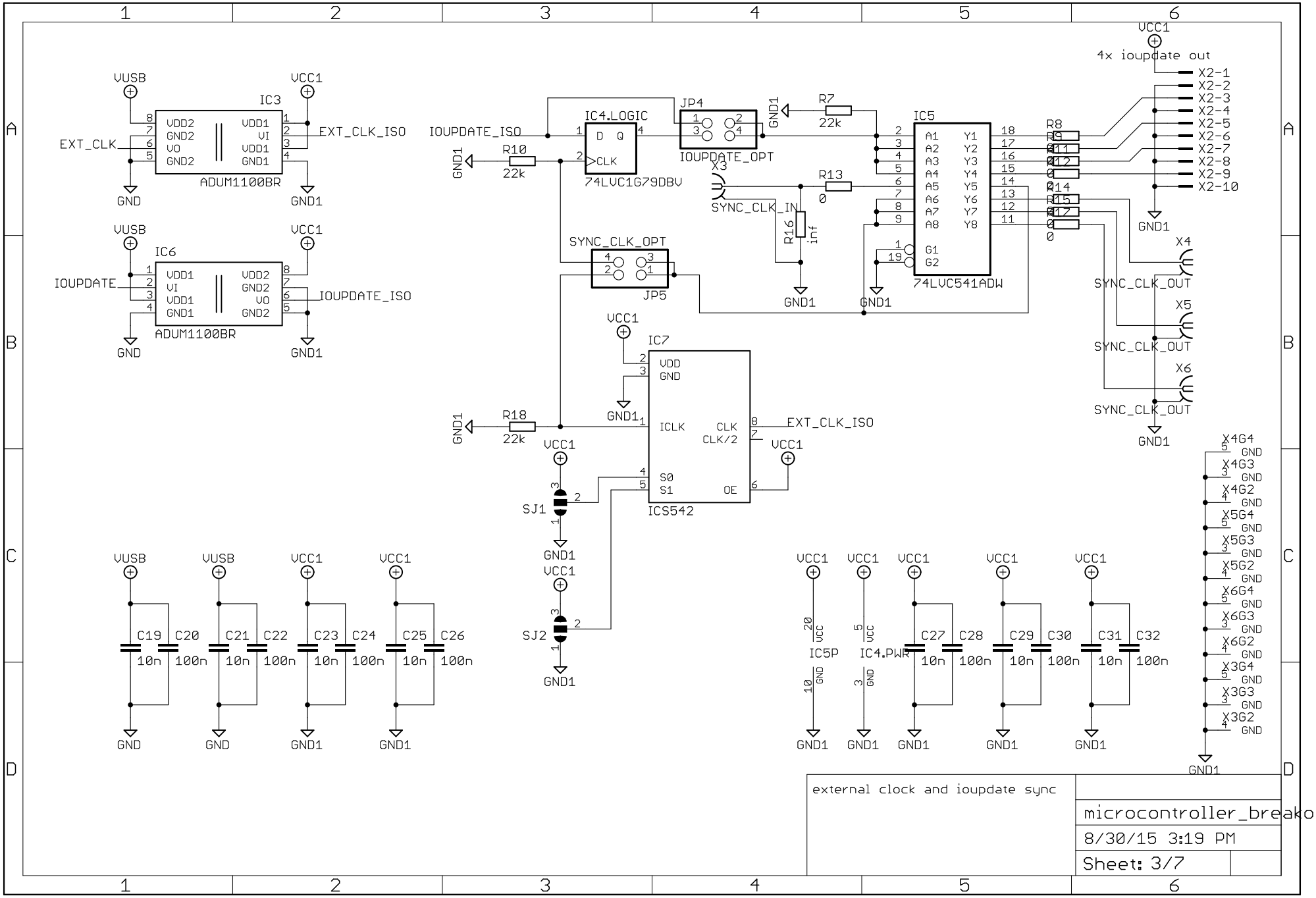
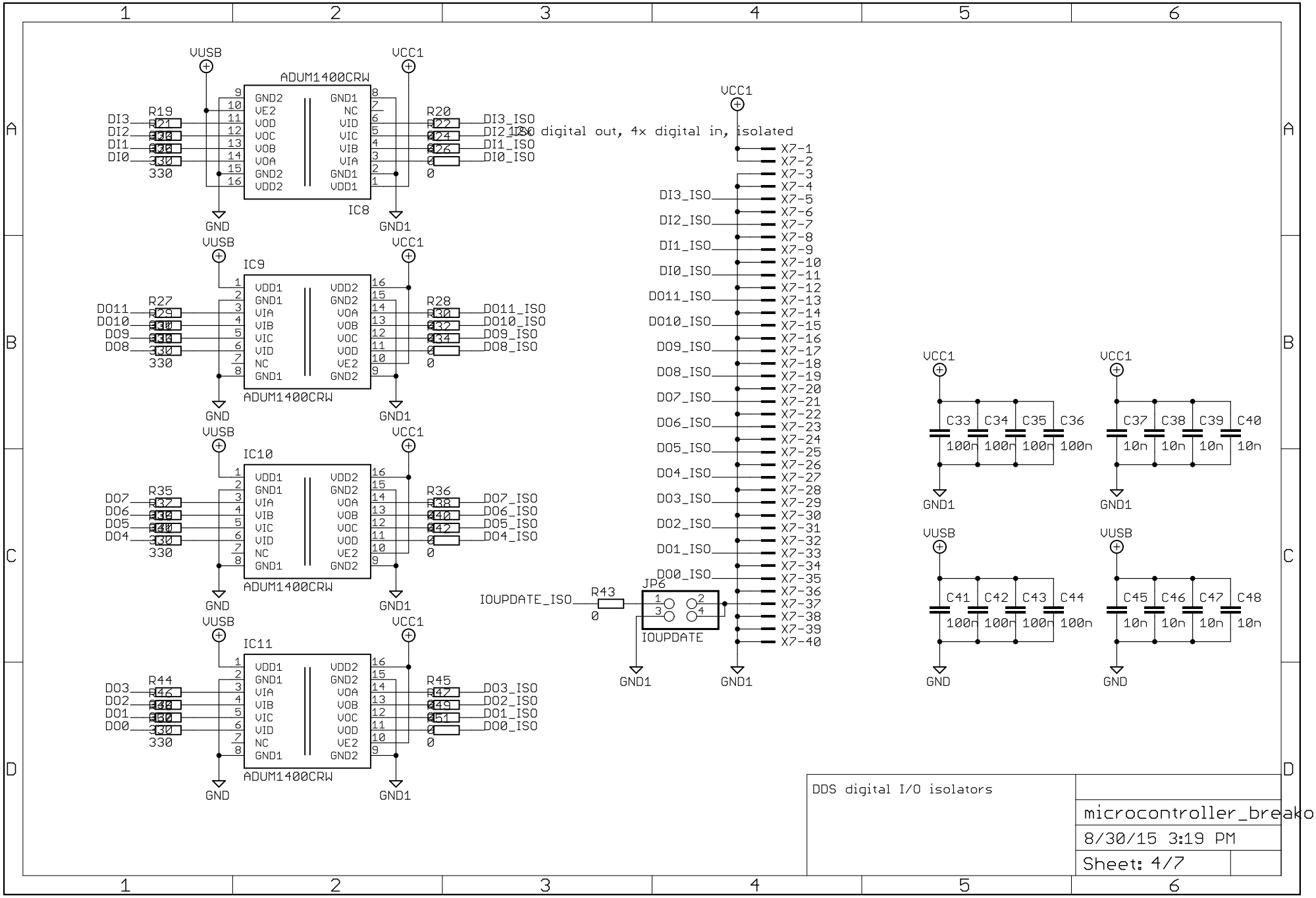
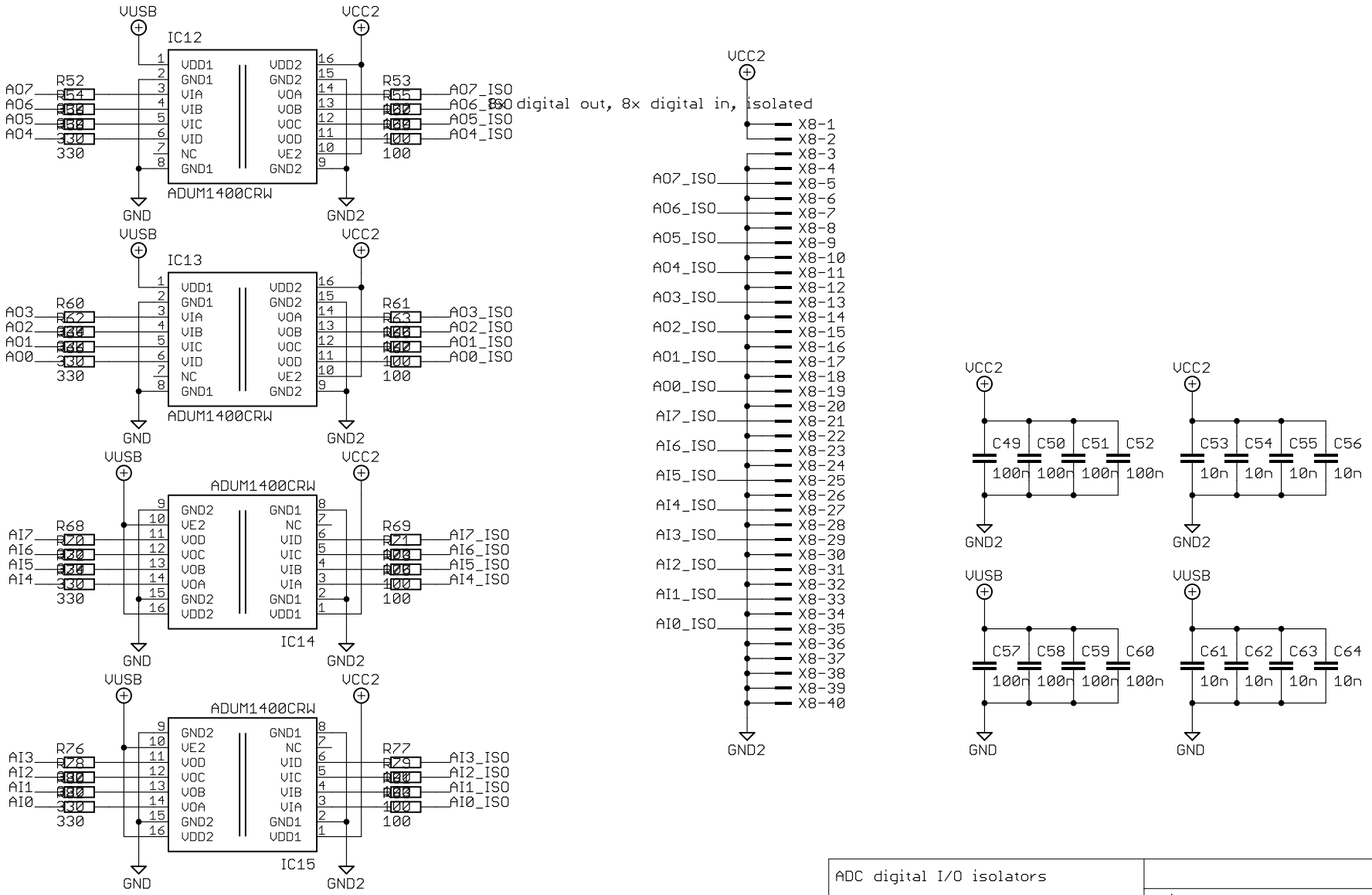
(AD0)PA0 78
(OC0A/OC1C/PCINT7)PB7 26 LED
(OC1B/PCINT6)PB6 25
(OC1A/PCINT5)PB5 24
(OC2A/PCINT4)PB4 23
(MISO/PCINT3)PB3 22 MISO
(MOSI/PCINT2)PB2 21 MOSI
(SCK/PCINT1)PB1 20 SCK
(SS/PCINT0)PB0 19
(A15)PC7 60 AI7
(A14)PC6 59 AI6
(A13)PC5 58 AI5
(A12)PC4 57 AI4
(A11)PC3 56 AI3
(A10)PC2 55 AI2
(A9)PC1 54 AI1
(A8)PC0 53 AI0
(T0)PD7 50 DI3
(T1)PD6 49 DI2
(XCK1)PD5 48 DI1
(ICP1)PD4 47 DI0
(TXD1/INT3)PD3 46 DO11
(RXD1/INT2)PD2 45 DO10
(SDA/INT1)PD1 44 DO9
(SCL/INT0)PD0 43 DO8
(CLKO/ICP3/INT7)PE7 9
(T3/INT6)PE6 8
(OC3C/INT5)PE5 7 XI3
(OC3B/INT4)PE4 6 XI2
(OC3A/AIN1)PE3 5
(XCK0/AIN0)PE2 4
(TXD0)PE1 3 TXD
(RXD0/PCIN8)PE0 2 RXD
(ADC7/TDI)PF7 90
(ADC6/TDO)PF6 91
(ADC5/TMS)PF5 92
(ADC4/TCK)PF4 93
(ADC3)PF3 94
(ADC2)PF2 95
(ADC1)PF1 96
(ADC0)PF0 97
(OC0B)PG5 1
(TOSC1)PG4 29
(TOSC2)PG3 28 IOUPDATE
(ALE)PG2 70
(RD)PG1 52
(WR)PG0 51
PL7 42
PL6 41
PL5(OC5C) 40
PL4(OC5B) 39
PL3(OC5A) 38
PL2(T5) 37
PL1(ICP5) 36
PL0(ICP4) 35
PK7(ADC15/PCINT23) 82
PK6(ADC14/PCINT22) 83
PK5(ADC13/PCINT21) 84
PK4(ADC12/PCINT20) 85
PK3(ADC11/PCINT19) 86
PK2(ADC10/PCINT18) 87
PK1(ADC9/PCINT17) 88
PK0(ADC8/PCINT16) 89
PJ7 79
PJ6(PCINT15) 69
PJ5(PCINT14) 68
PJ4(PCINT13) 67
PJ3(PCINT12) 66
PJ2(XCK3/PCINT11) 65
PJ1(TXD3/PCINT10) 64
PJ0(RXD3/PCINT9) 63
PH7(T4) 27
PH6(OC2B) 18
PH5(OC4C) 17
PH4(OC4B) 16
PH3(OC4A) 15
PH2(XCK2) 14
PH1(TXD2) 13
PH0(RXD2) 12
JP3
ISP
MISO
SCK
RESET
MOSI
VUSB
GND
LED
R6 270
LED3 GREEN
AREF
C13 100n
C14 100n
C15 100n
C16 100n
C17 100n
C18 100n
microcontroller
microcontroller_breakout
8/30/15 3:19 PM
Sheet: 2/7


IC3
ADUM1100BR
VDD2
GND2
VO
GND2
VDD1
VI
VDD1
GND1
VUSB
VCC1
EXT_CLK
EXT_CLK_ISO
GND
GND1
IC6
ADUM1100BR
IOUPDATE
IOUPDATE_ISO
IC4.LOGIC
74LVC1G79DBV
D Q
CLK
IOUPDATE_ISO
R10
22k
JP4
IOUPDATE_OPT
R7
22k
IC5
74LVC541ADW
A1 A2 A3 A4 A5 A6 A7 A8
Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8
G1 G2
R8 R9 R11 R12 R14 R15 R17
X3
SYNC_CLK_IN
R13
0
R16
inf
SYNC_CLK_OPT
JP5
4x ioupdate out
X2-1 X2-2 X2-3 X2-4 X2-5 X2-6 X2-7 X2-8 X2-9 X2-10
X4
X5
X6
SYNC_CLK_OUT
IC7
ICS542
VDD
GND
ICLK
CLK
CLK/2
S0
S1
OE
R18
22k
EXT_CLK_ISO
SJ1
SJ2
C19 C20 C21 C22 C23 C24 C25 C26
10n 100n
IC5P
IC4.PWR
C27 C28 C29 C30 C31 C32
X4G4 X4G3 X4G2 X5G4 X5G3 X5G2 X6G4 X6G3 X6G2 X3G4 X3G3 X3G2
external clock and ioupdate sync
microcontroller_breakout
8/30/15 3:19 PM
Sheet: 3/7


ADUM1400CRW
IC8
IC9
IC10
IC11
VUSB
VCC1
GND
GND1
R19
R20
R27
R28
R35
R36
R44
R45
330
0
DI3_ISO
DI2_ISO
DI1_ISO
DI0_ISO
DO11_ISO
DO10_ISO
DO9_ISO
DO8_ISO
DO7_ISO
DO6_ISO
DO5_ISO
DO4_ISO
DO3_ISO
DO2_ISO
DO1_ISO
DO0_ISO
IOUPDATE_ISO
R43
JP6
IOUPDATE
X7-1
X7-2
X7-3
X7-4
X7-5
X7-6
X7-7
X7-8
X7-9
X7-10
X7-11
X7-12
X7-13
X7-14
X7-15
X7-16
X7-17
X7-18
X7-19
X7-20
X7-21
X7-22
X7-23
X7-24
X7-25
X7-26
X7-27
X7-28
X7-29
X7-30
X7-31
X7-32
X7-33
X7-34
X7-35
X7-36
X7-37
X7-38
X7-39
X7-40
C33 C34 C35 C36
100n
C37 C38 C39 C40
10n
C41 C42 C43 C44
100n
C45 C46 C47 C48
10n
DDS digital I/O isolators
microcontroller_breakout
8/30/15 3:19 PM
Sheet: 4/7

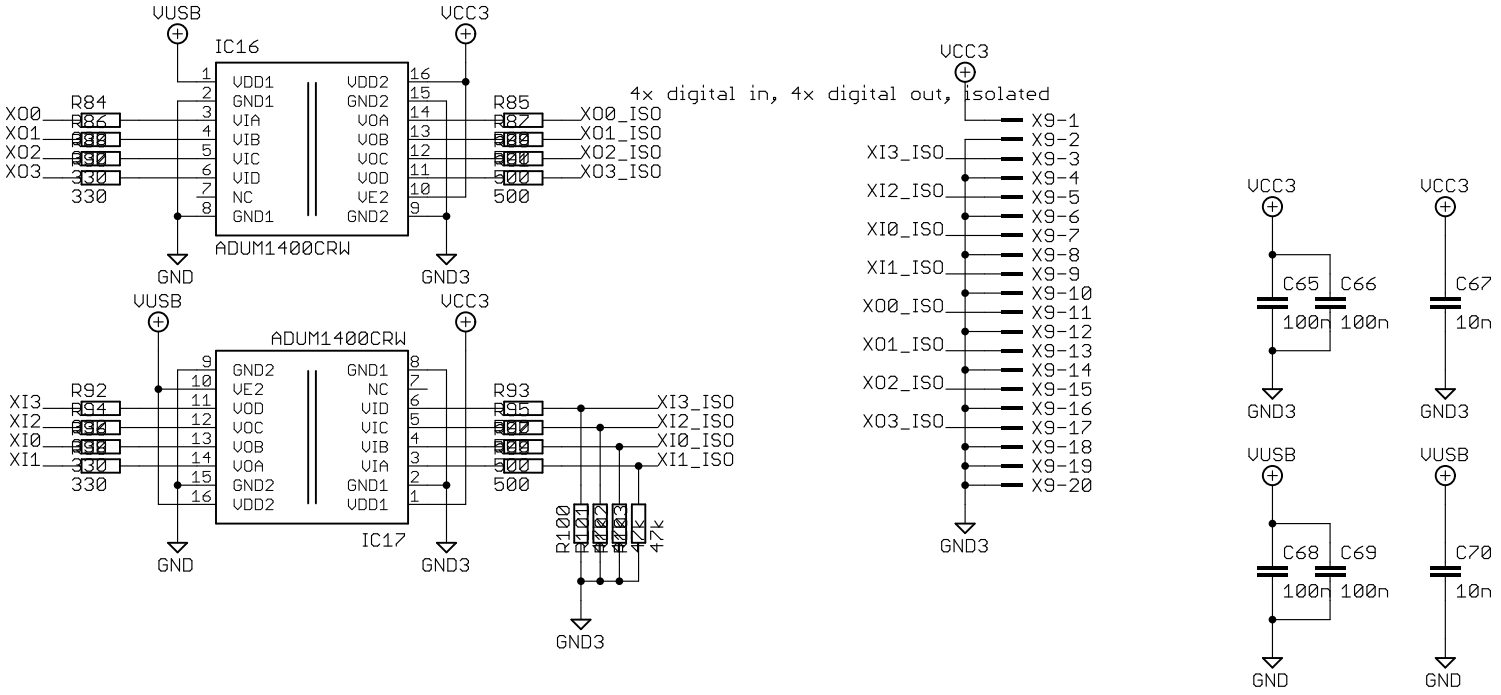


ADC digital I/O isolators

microcontroller_breakout

8/30/15 3:19 PM

Sheet: 5/7

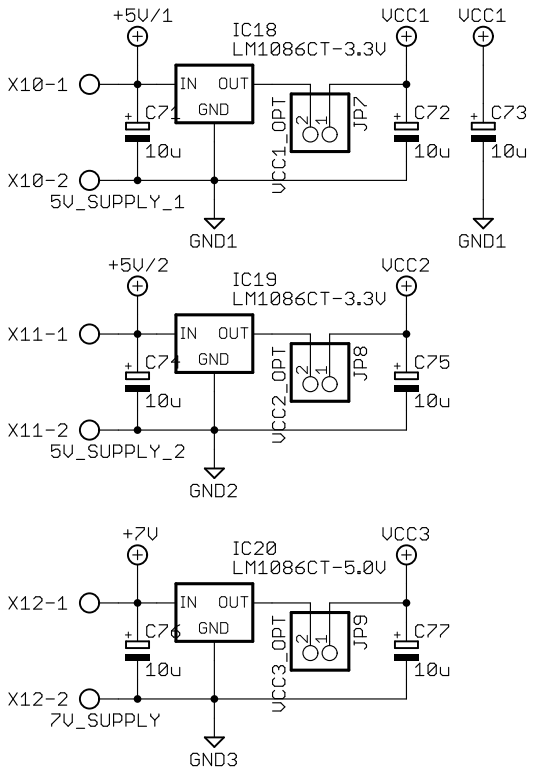


external digital I/O isolators

microcontroller_breakout

8/30/15 3:19 PM

Sheet: 6/7

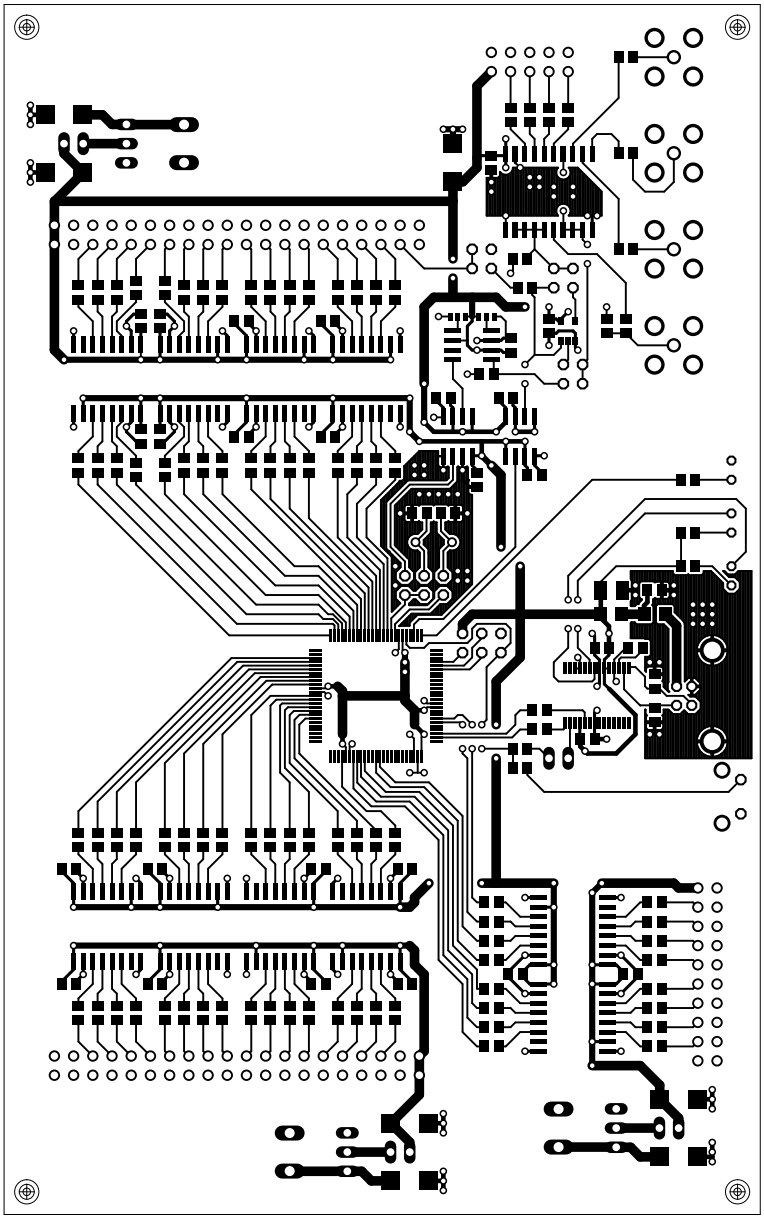


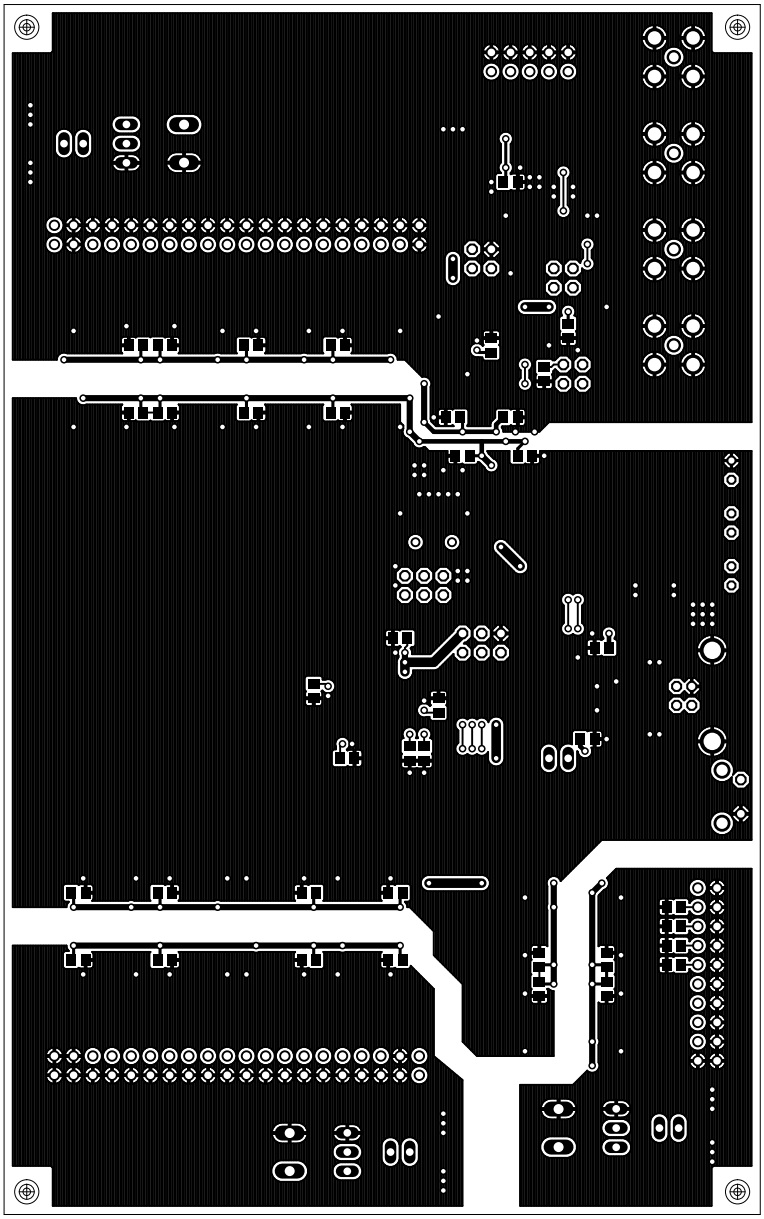
power supplies

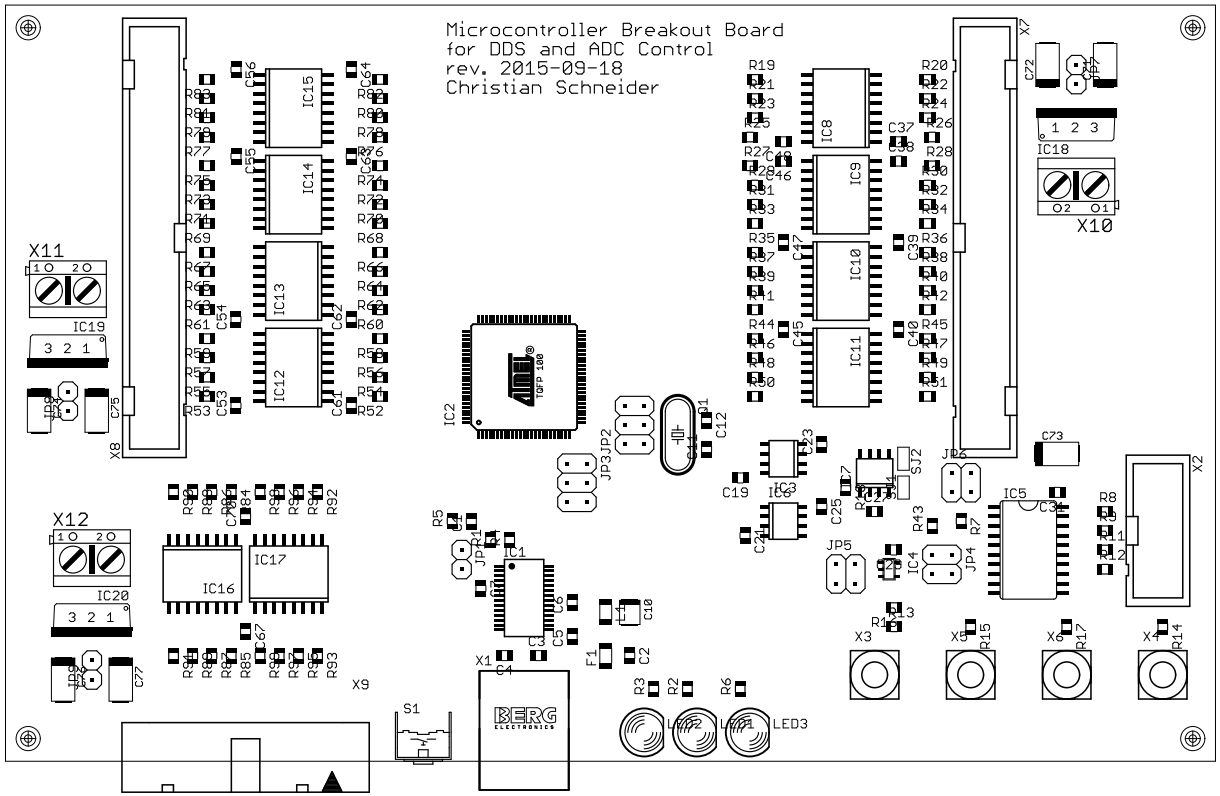
microcontroller_breakout

8/30/15 3:19 PM

Sheet: 7/7

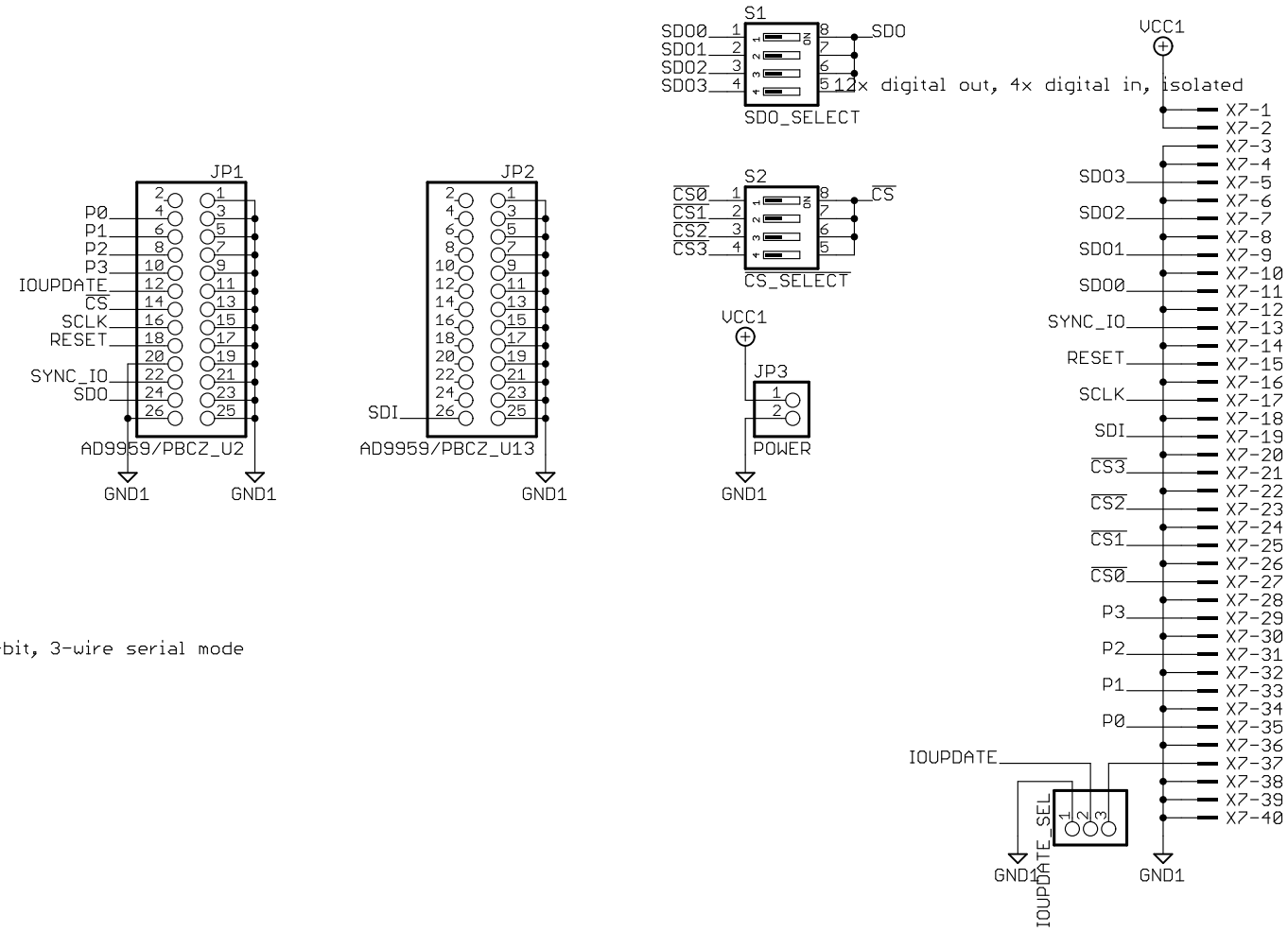





Microcontroller Breakout Board
for DDS and ADC Control
rev. 2015-09-18
Christian Schneider
X11
X12
IC19
IC20
IC18
X10
X8
X9
X7
X2
X1
IC1
IC2
IC3
IC4
IC5
IC8
IC9
IC10
IC11
IC12
IC13
IC14
IC15
IC16
IC17
JP3
JP2
JP4
JP5
S1
F1
LED1
LED2
LED3
X3
X4
X5
X6
BERG
ELECTRONICS

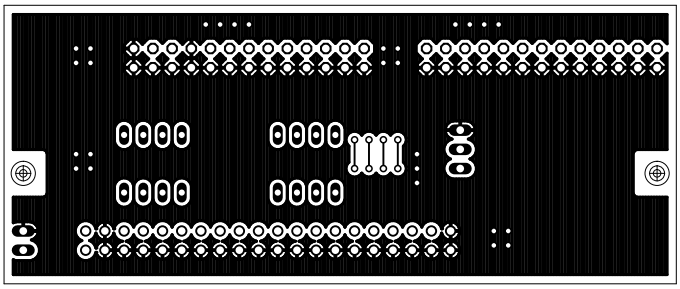
C32
C38
RT9
C27
C33
C34
C35
C36
C24
C41
C42
C43
C44
C20
C26
C22
C45
C9
C16
C14
C8
C13
C7
C8
C60
C59
C58
C57
C52
C51
C50
C49
C28
C25
C29
C26
R103
R102
R101
R100

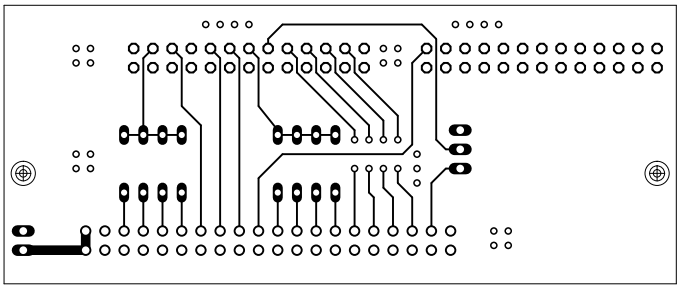
A.2. DDS Chain Board



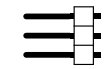
signal names refer to single-bit, 3-wire serial mode

dds_chain	
6/7/13 1:28 PM	
Sheet: 1/1	



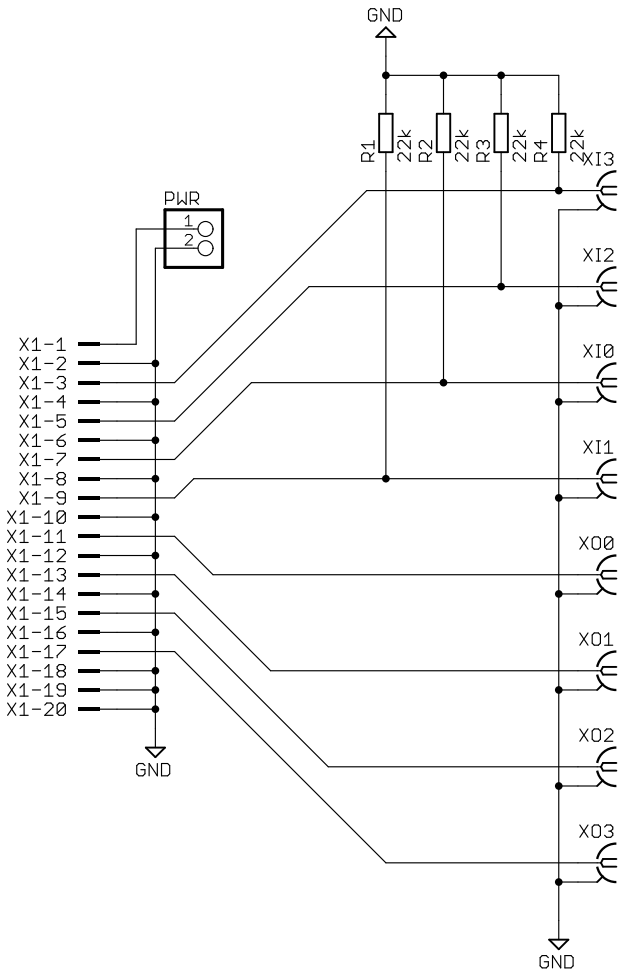


AD9959/PBCZ Chain Board
rev. 2013-06-03



JP2
JP1
ON
1 2 3 4
S2
ON
1 2 3 4
S1
LB3
X1

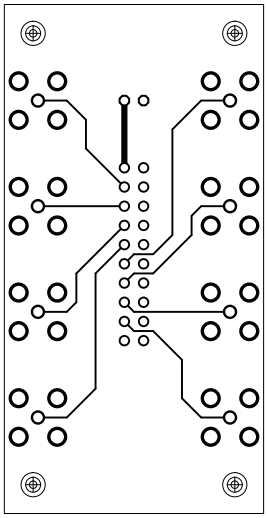
A.3. External I/O Breakout Board

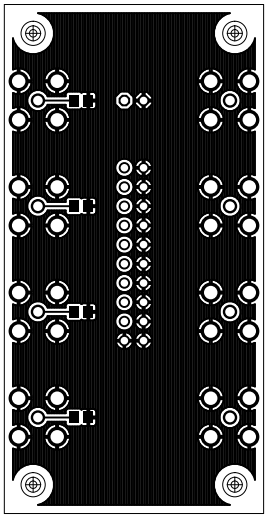


digital_io_breakout

10/11/13 12:07 PM

Sheet: 1/1

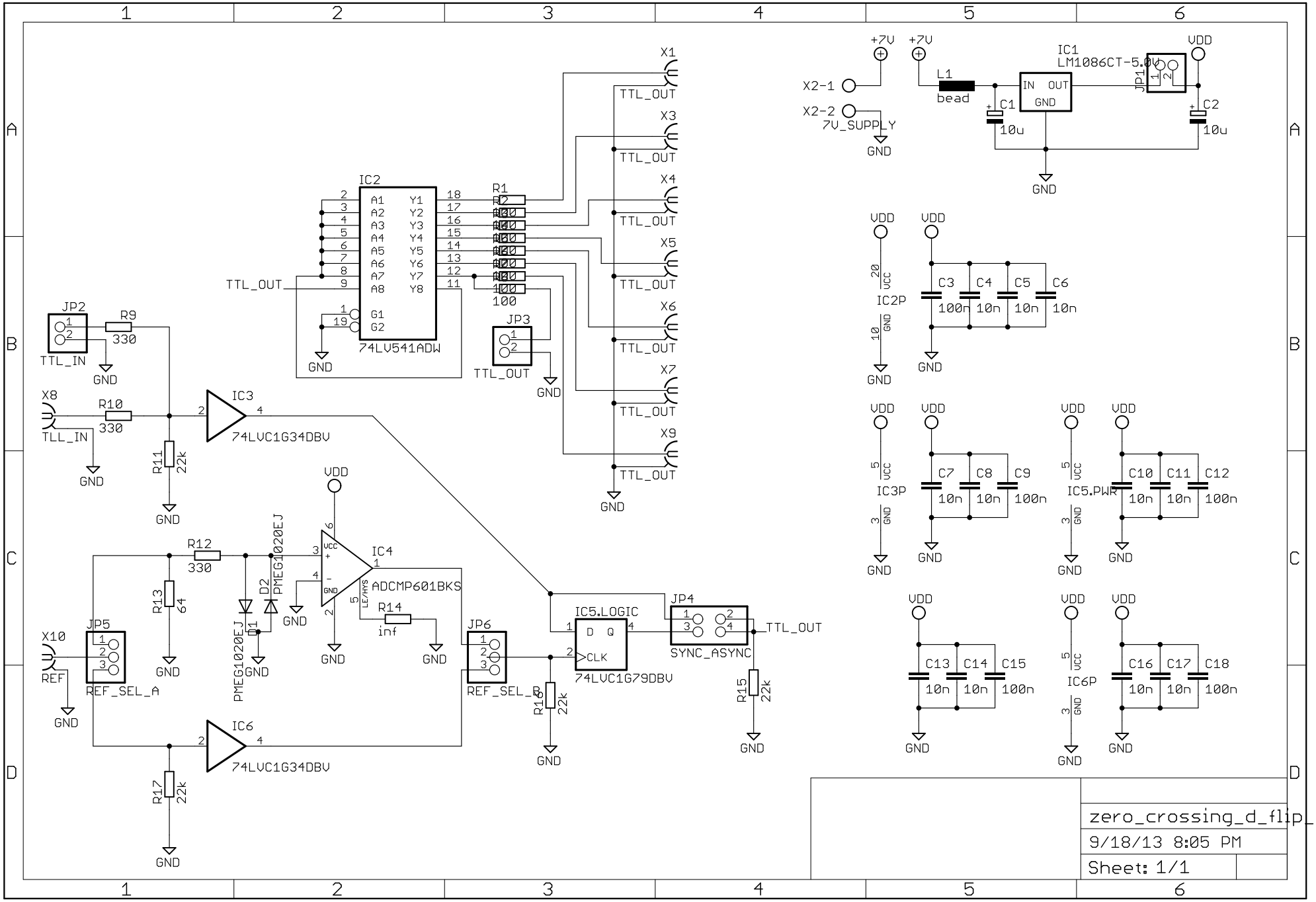


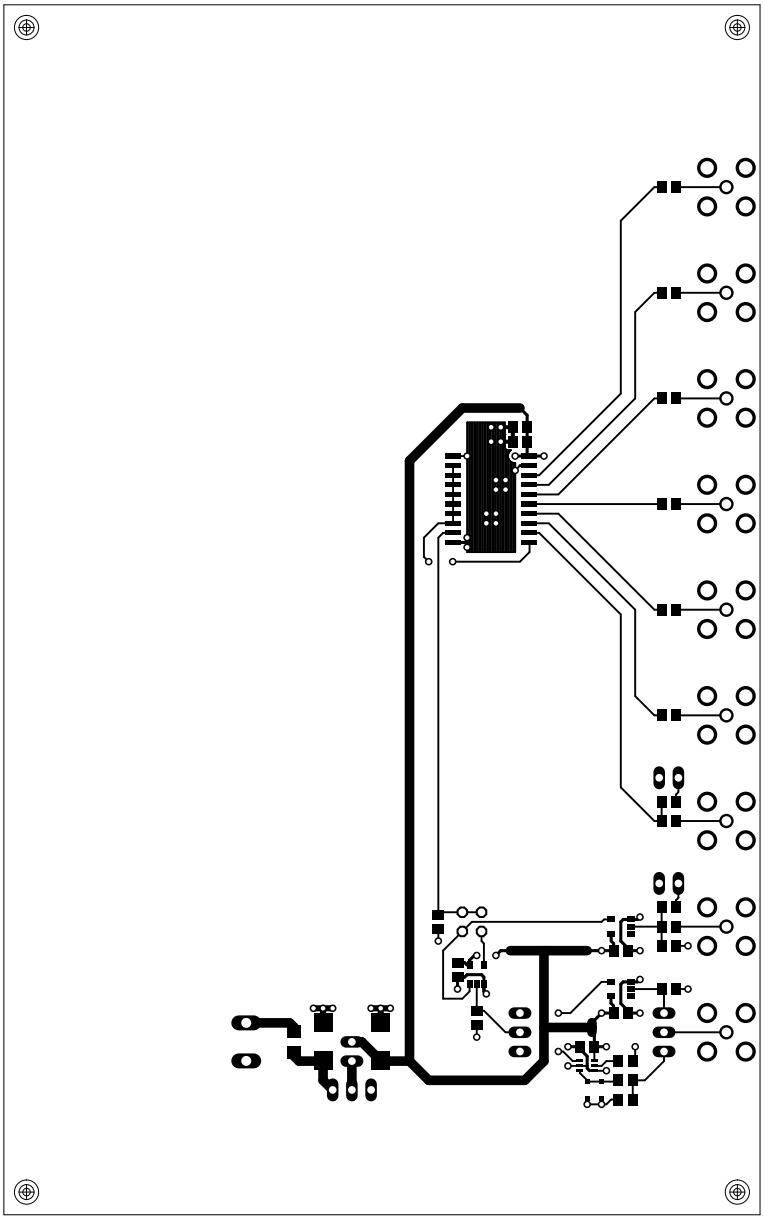


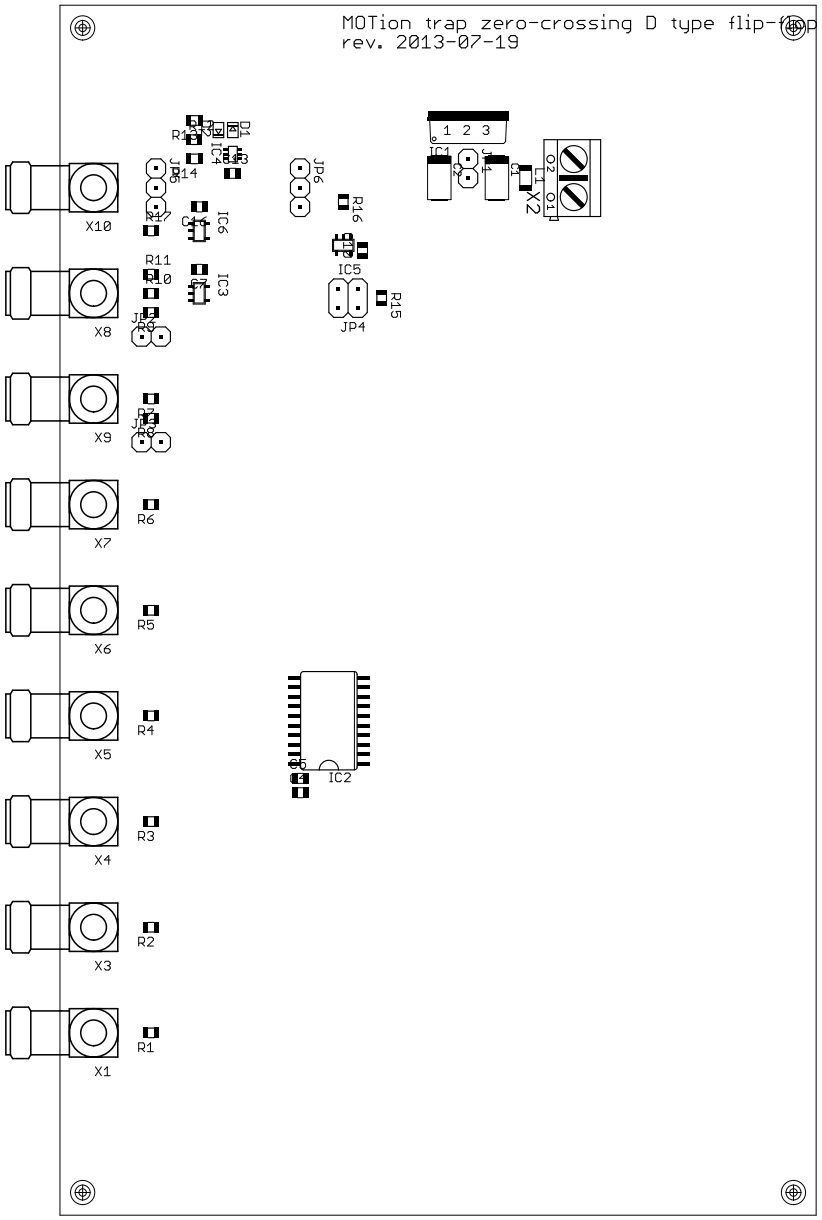
digital I/O breakout
rev. 2013-10-11
INPUTS
OUTPUTS
X1
PWR
XI1
XI0
XI2
XI3
XO3
XO2
XO1
XO0

R1
R2
R3
R4

A.4. Zero-Crossing D-Type Flip-Flop

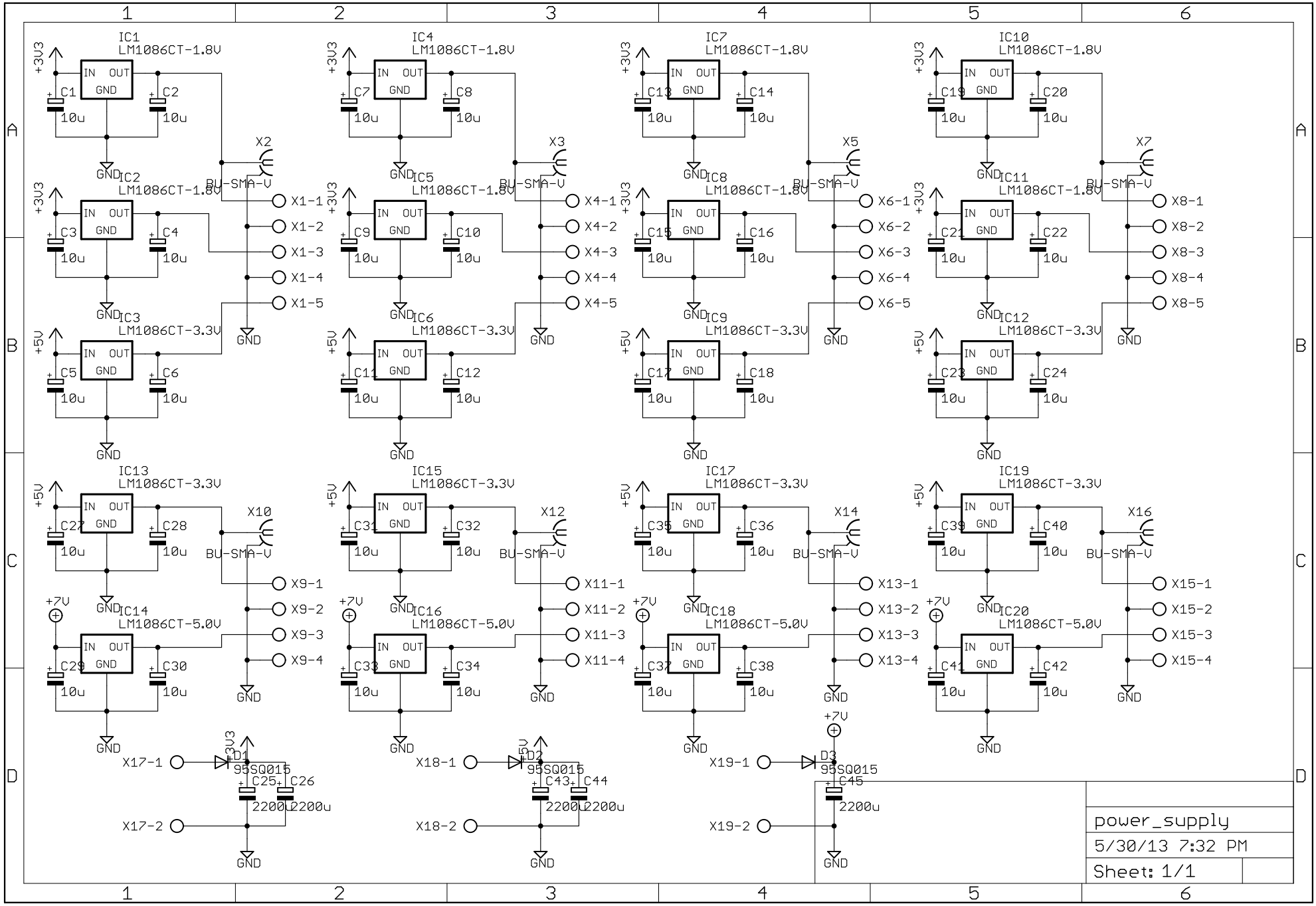

IC2
74LV541ADW
A1 A2 A3 A4 A5 A6 A7 A8
Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8
G1 G2
R1
100
TTL_OUT
X1 X3 X4 X5 X6 X7 X9
JP2
TTL_IN
R9
330
JP3
X8
TLL_IN
R10
330
IC3
74LVC1G34DBV
R11
22k
VDD
R12
330
PMEG1020EJ
D2
D1
IC4
ADCMP601BKS
VCC
GND
LE/HYS
R14
inf
R13
64
X10
REF
JP5
REF_SEL_A
JP6
REF_SEL_B
IC6
74LVC1G34DBV
R17
22k
IC5.LOGIC
D Q
CLK
74LVC1G79DBV
R16
22k
JP4
SYNC_ASYNC
R15
22k
GND
+7V
X2-1
X2-2
7V_SUPPLY
L1
bead
C1
10u
IC1
LM1086CT-5.0V
IN OUT
JP1
C2
10u
IC2P
C3 C4 C5 C6
100n 10n 10n 10n
IC3P
C7 C8 C9
10n 10n 100n
IC5.PWR
C10 C11 C12
10n 10n 100n
C13 C14 C15
10n 10n 100n
IC6P
C16 C17 C18
10n 10n 100n
zero_crossing_d_flip_flop
9/18/13 8:05 PM
Sheet: 1/1

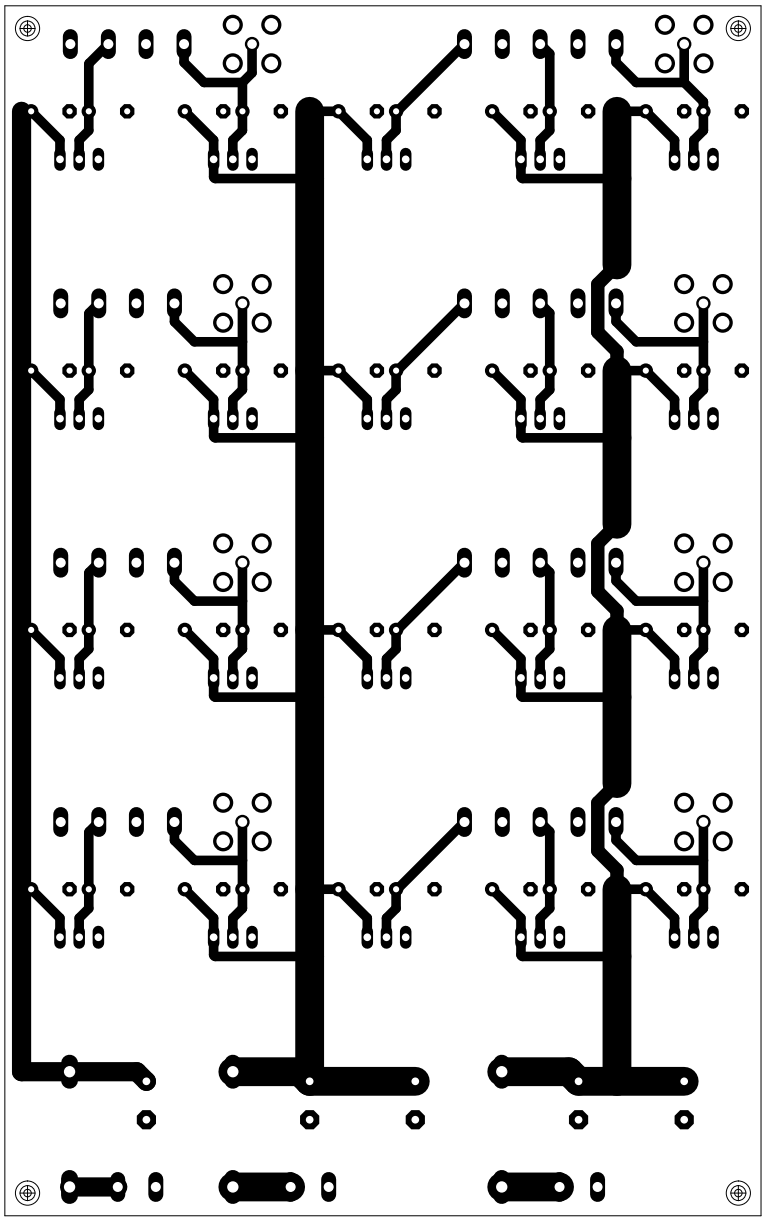


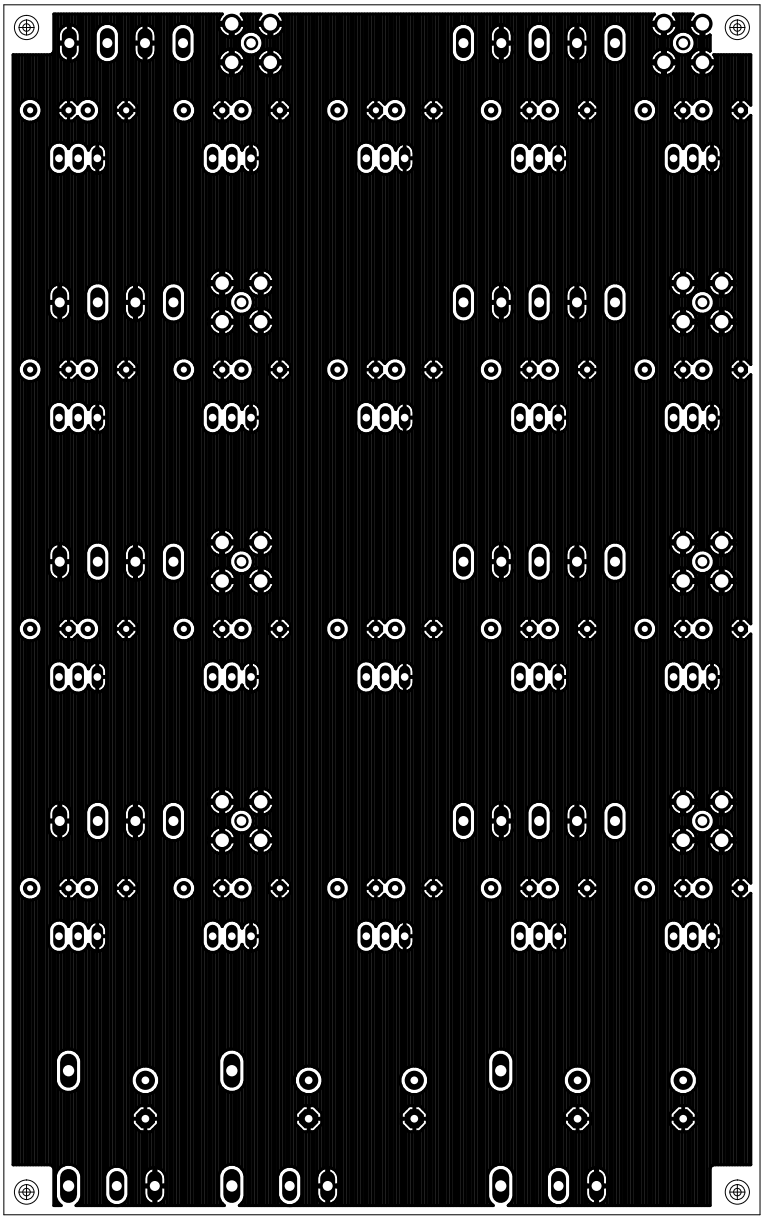

MOTion trap zero-crossing D type flip-flop
rev. 2013-07-19
X10
X8
X9
X7
X6
X5
X4
X3
X1
R1
R2
R3
R4
R5
R6
R11
R10
R14
R17
R16
R15
D1
IC4
IC6
IC3
IC5
IC2
IC1
JP6
JP4
JP5
JP9
JP1
C1
C2
L1
Y2
O1
O2
1 2 3

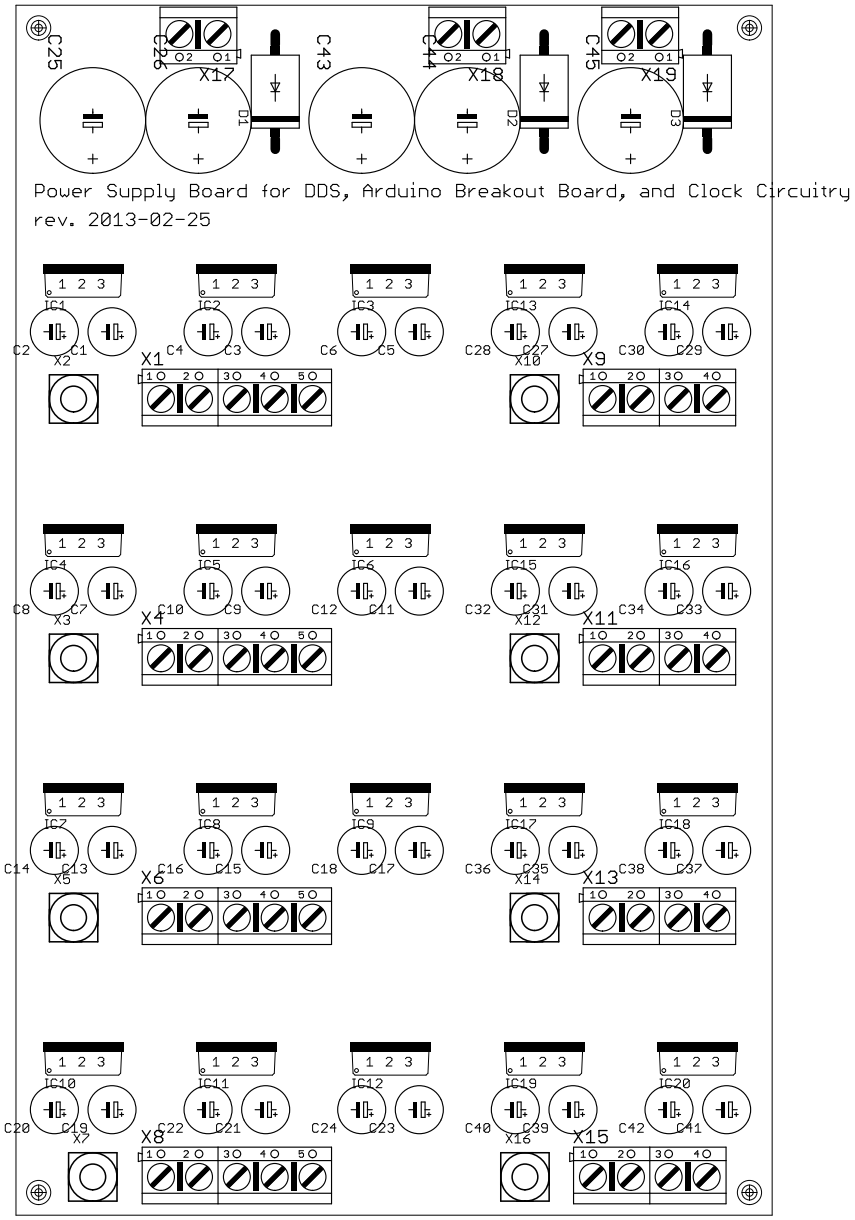
C3
C8
C12
C14
C17
C24

A.5. Power Supply Board


IC1 LM1086CT-1.8V
IC2 LM1086CT-1.8V
IC3 LM1086CT-3.3V
IC4 LM1086CT-1.8V
IC5 LM1086CT-1.8V
IC6 LM1086CT-3.3V
IC7 LM1086CT-1.8V
IC8 LM1086CT-1.8V
IC9 LM1086CT-3.3V
IC10 LM1086CT-1.8V
IC11 LM1086CT-1.8V
IC12 LM1086CT-3.3V
IC13 LM1086CT-3.3V
IC14 LM1086CT-5.0V
IC15 LM1086CT-3.3V
IC16 LM1086CT-5.0V
IC17 LM1086CT-3.3V
IC18 LM1086CT-5.0V
IC19 LM1086CT-3.3V
IC20 LM1086CT-5.0V
IN OUT GND
+3V3
+5V
+7V
GND
10u
X1-1 X1-2 X1-3 X1-4 X1-5
X2 X3 X5 X7
BU-SMA-V
X4-1 X4-2 X4-3 X4-4 X4-5
X6-1 X6-2 X6-3 X6-4 X6-5
X8-1 X8-2 X8-3 X8-4 X8-5
X9-1 X9-2 X9-3 X9-4
X10 X12 X14 X16
X11-1 X11-2 X11-3 X11-4
X13-1 X13-2 X13-3 X13-4
X15-1 X15-2 X15-3 X15-4
X17-1 X17-2
X18-1 X18-2
X19-1 X19-2
D1 D2 D3
95SQ015
2200u
power_supply
5/30/13 7:32 PM
Sheet: 1/1

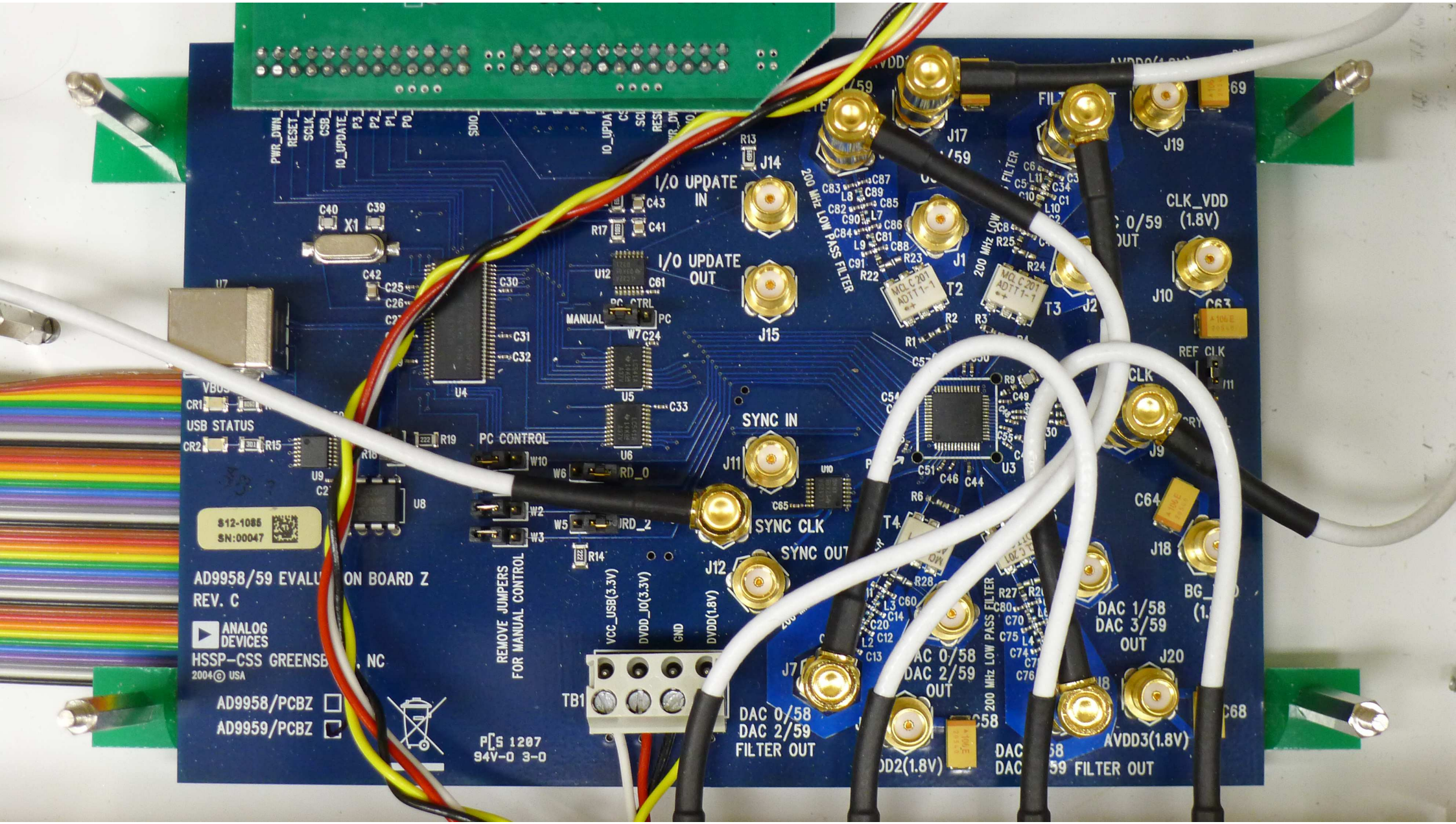


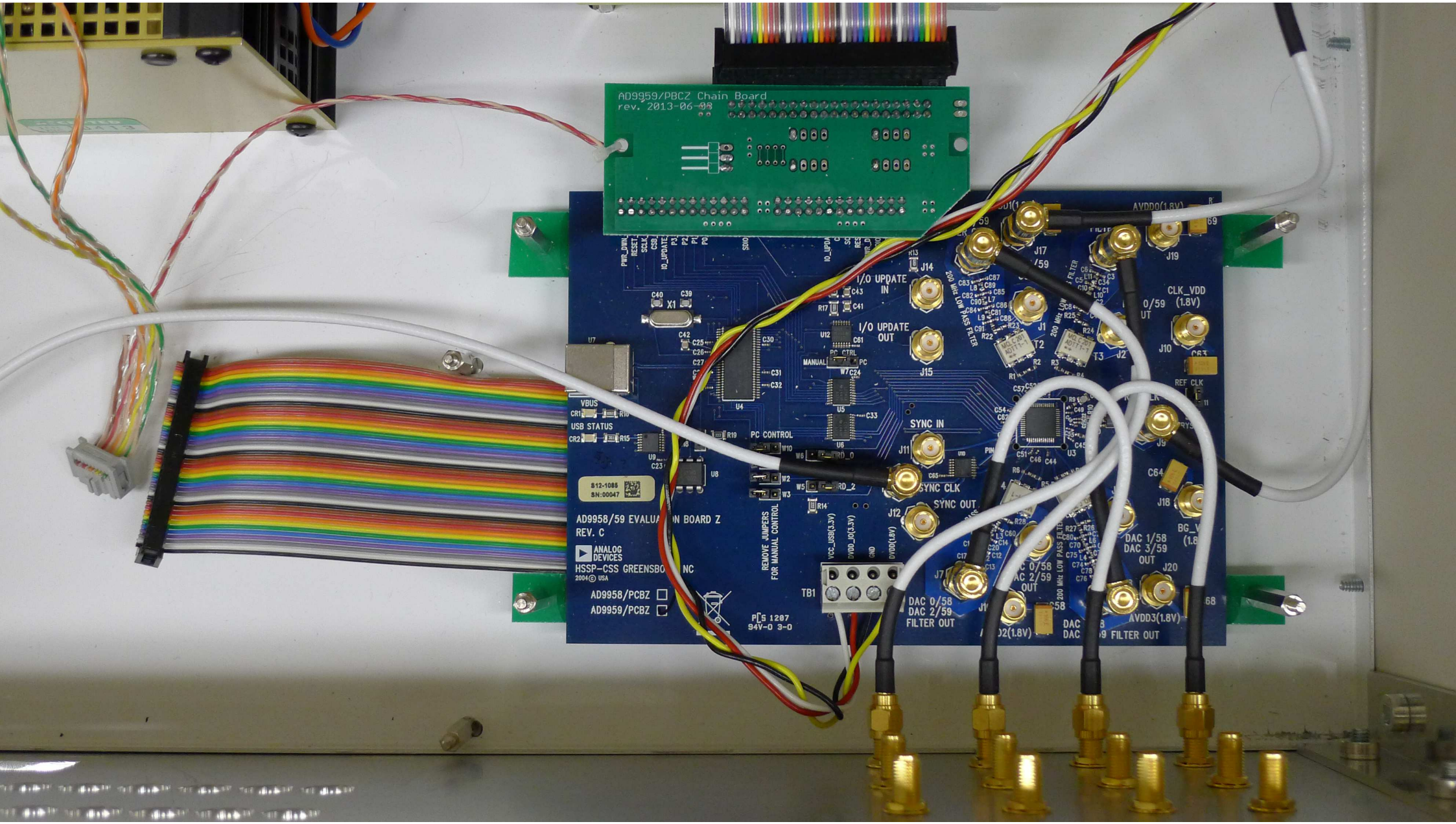


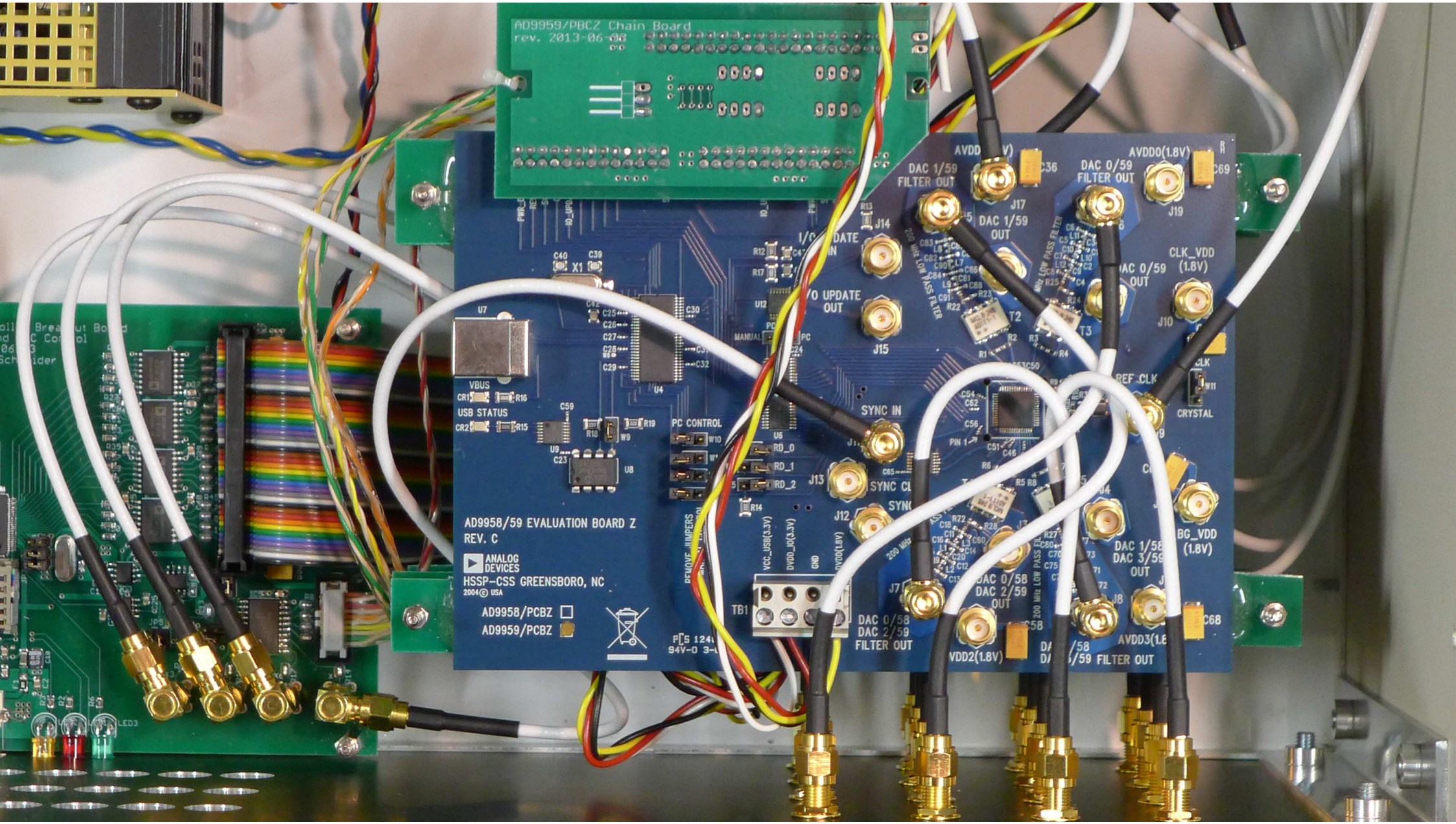

C25
C26
X17
C43
C44
X18
C45
X19
D1
D2
D3
Power Supply Board for DDS, Arduino Breakout Board, and Clock Circuitry
rev. 2013-02-25
IC1
IC2
IC3
IC13
IC14
C2
C1
C4
C3
C6
C5
C28
C27
C30
C29
X2
X1
X10
X9
IC4
IC5
IC6
IC15
IC16
C8
C7
C10
C9
C12
C11
C32
C31
C34
C33
X3
X4
X12
X11
IC7
IC8
IC9
IC17
IC18
C14
C13
C16
C15
C18
C17
C36
C35
C38
C37
X5
X6
X14
X13
IC10
IC11
IC12
IC19
IC20
C20
C19
C22
C21
C24
C23
C40
C39
C42
C41
X7
X8
X16
X15

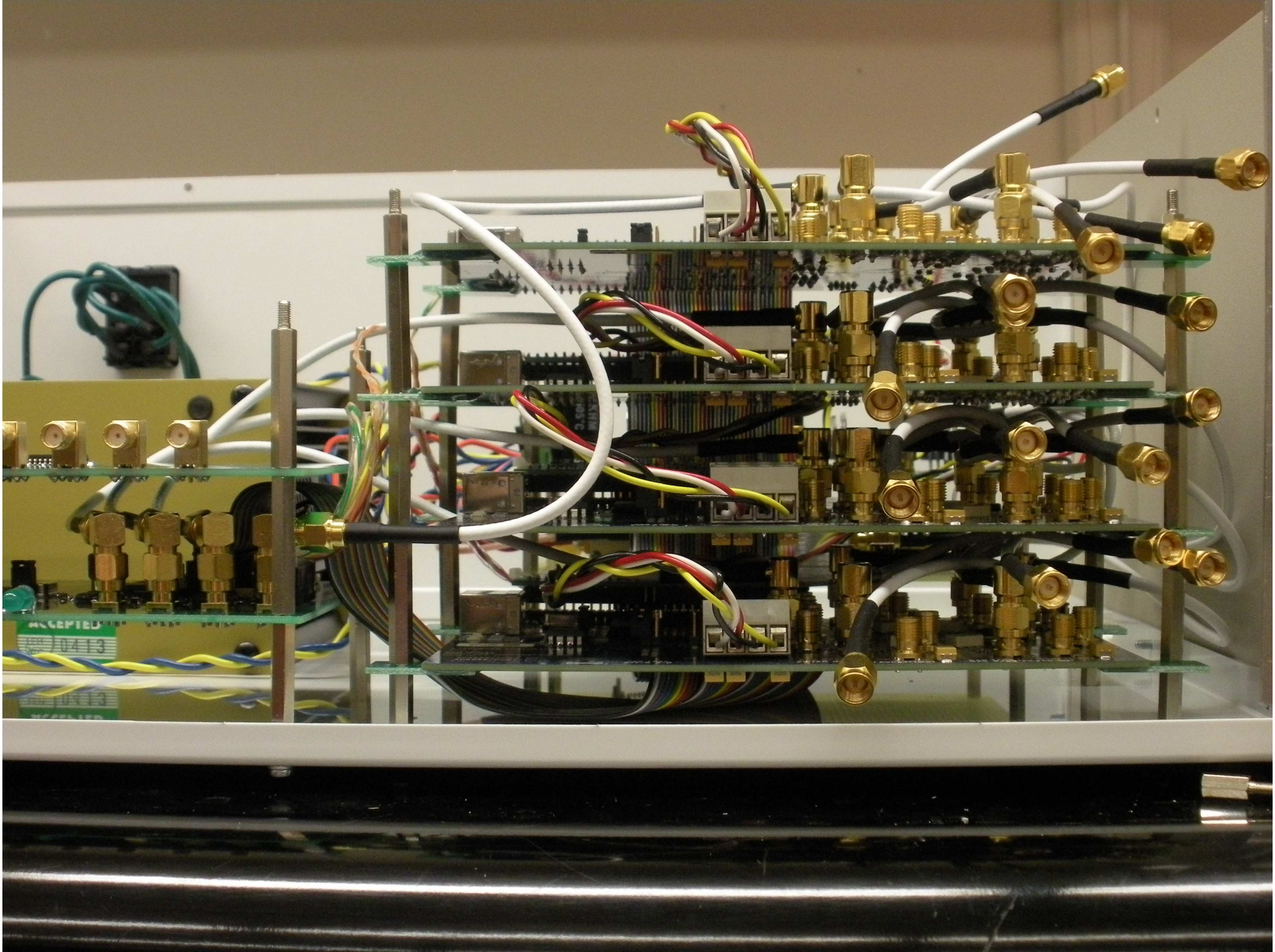
B. Photographs

B.1. DDS Boards

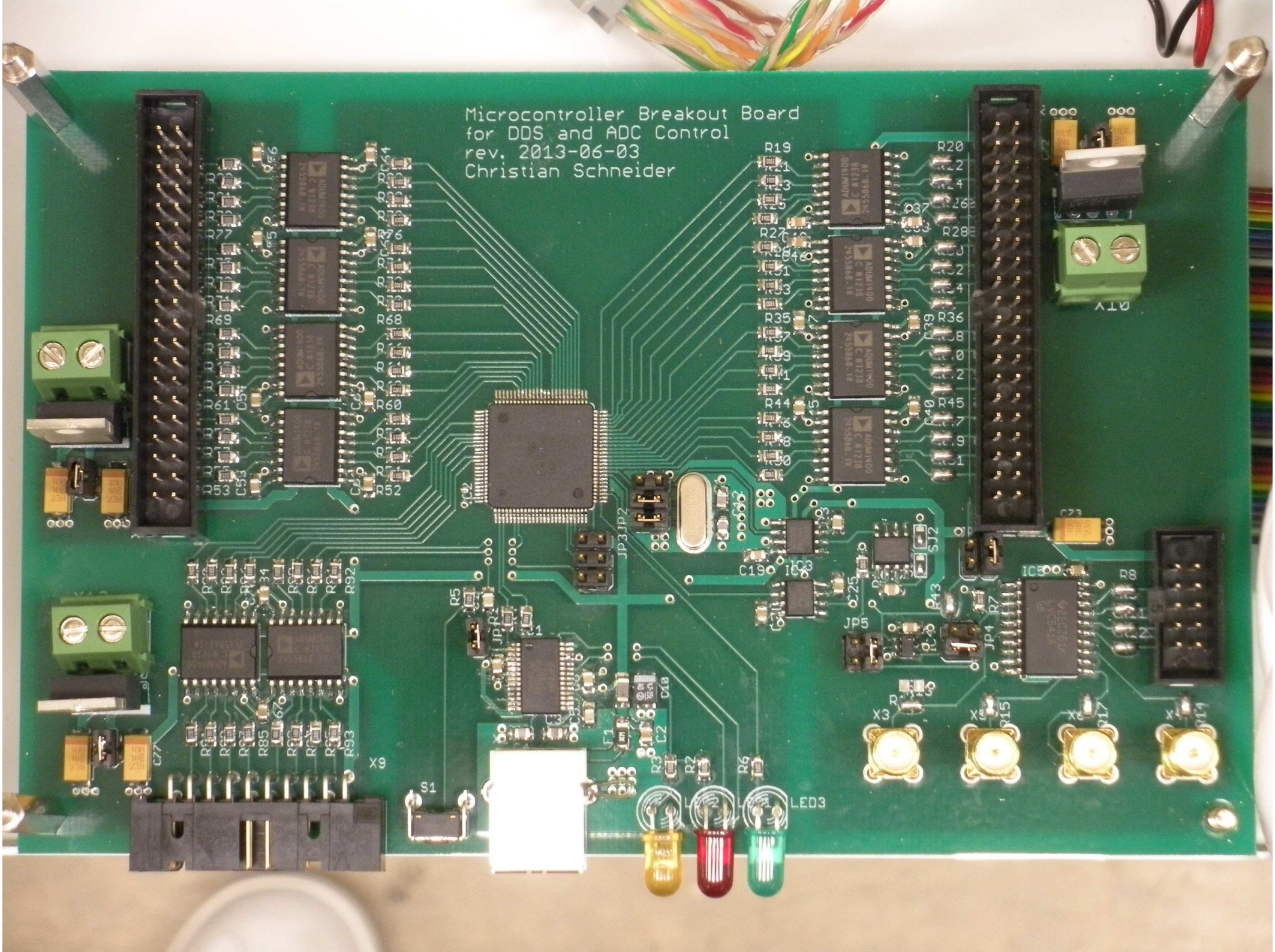

I/O UPDATE IN
I/O UPDATE OUT
SYNC IN
SYNC CLK
SYNC OUT
CLK_VDD (1.8V)
REF CLK
USB STATUS
PC CONTROL
MANUAL
PC
REMOVE JUMPERS FOR MANUAL CONTROL
VCC_USB(3.3V)
DVDD_IO(3.3V)
GND
DVDD(1.8V)
TB1
AD9958/59 EVALU ON BOARD Z
REV. C
ANALOG DEVICES
HSSP-CSS GREENSB , NC
2004© USA
AD9958/PCBZ
AD9959/PCBZ
S12-1085
SN:00047
DAC 0/58
DAC 2/59
FILTER OUT
DAC 0/58
DAC 2/59
OUT
DAC 1/58
DAC 3/59
OUT
AVDD3(1.8V)
200 MHz LOW PASS FILTER

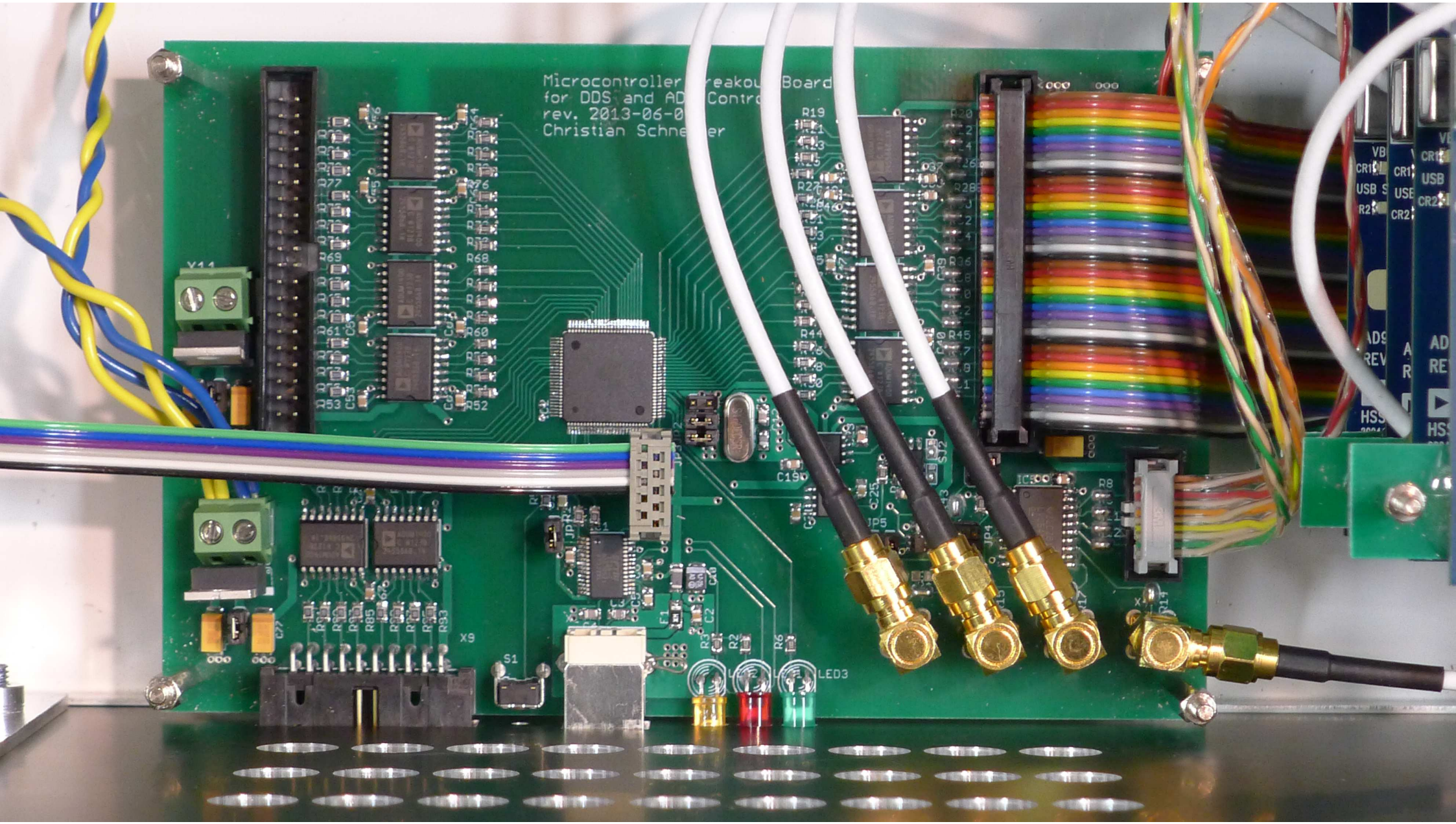

AD9959/PBCZ Chain Board
rev. 2013-06-08
I/O UPDATE IN
I/O UPDATE OUT
SYNC IN
SYNC CLK
SYNC OUT
PC CONTROL
USB STATUS
VBUS
REMOVE JUMPERS FOR MANUAL CONTROL
AD9958/59 EVALUATION BOARD Z
REV. C
ANALOG DEVICES
AD9958/PCBZ
AD9959/PCBZ
TB1
CLK_VDD (1.8V)
REF CLK
DAC 0/58 DAC 2/59 FILTER OUT
DAC 1/58 DAC 3/59 OUT
AVDD3(1.8V)


AD9959/PBCZ Chain Board
rev. 2013-06-08
AD9958/59 EVALUATION BOARD Z
REV. C
ANALOG DEVICES
HSSP-CSS GREENSBORO, NC
AD9958/PCBZ
AD9959/PCBZ
USB STATUS
PC CONTROL
SYNC IN
DAC 1/59 FILTER OUT
DAC 1/59 OUT
DAC 0/59 FILTER OUT
DAC 0/59 OUT
CLK_VDD (1.8V)
REF CLK
CRYSTAL
BG_VDD (1.8V)
DAC 0/58 DAC 2/59 FILTER OUT
DAC 0/58 DAC 2/59 OUT
DAC 1/58 DAC 3/59 OUT
AVDD0(1.8V)
AVDD2(1.8V)
AVDD3(1.8V)
TB1
VCC_USB(3.3V)
DVDD_IO(3.3V)
GND
DVDD(1.8V)

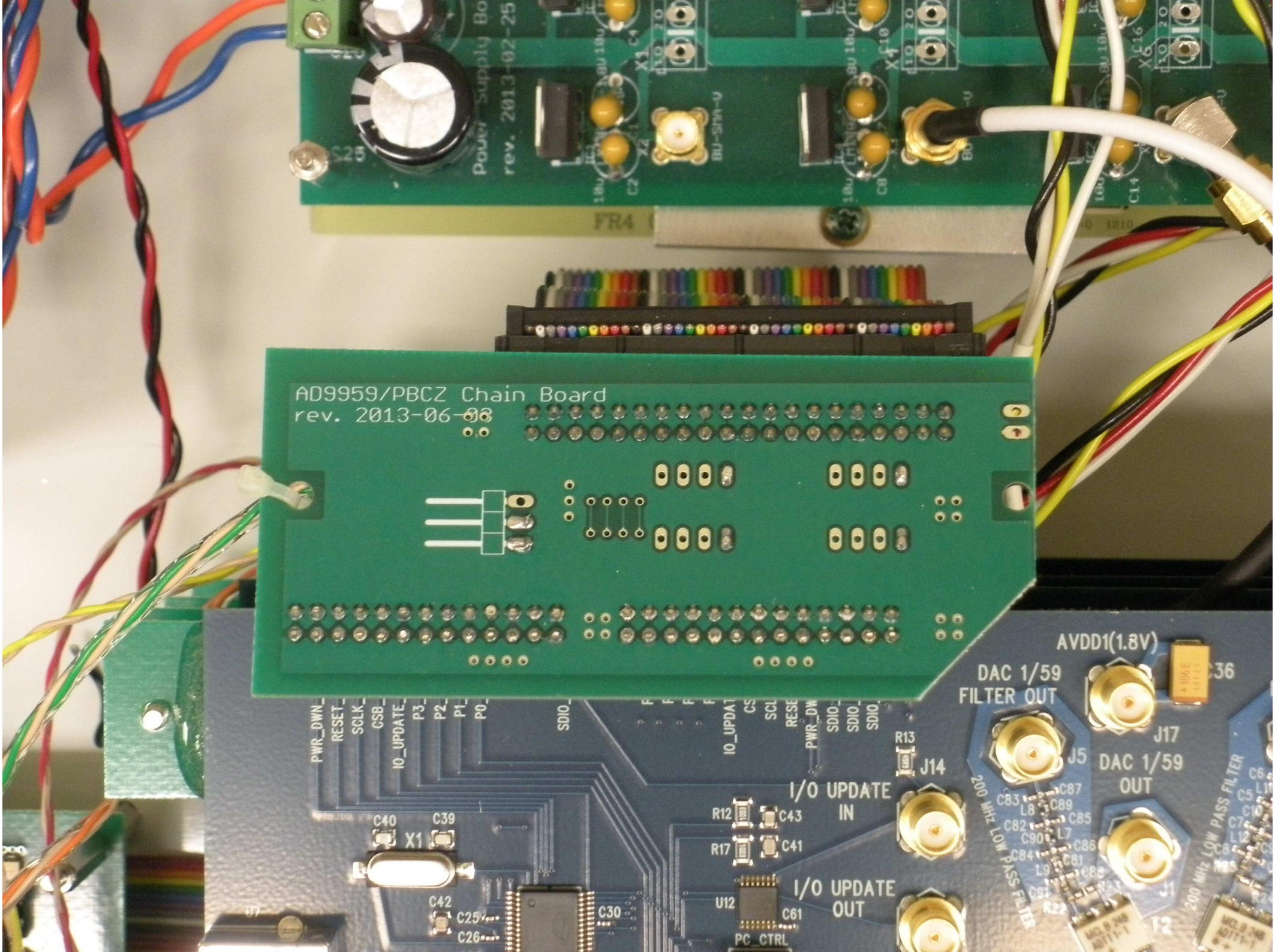

ACCEPTED

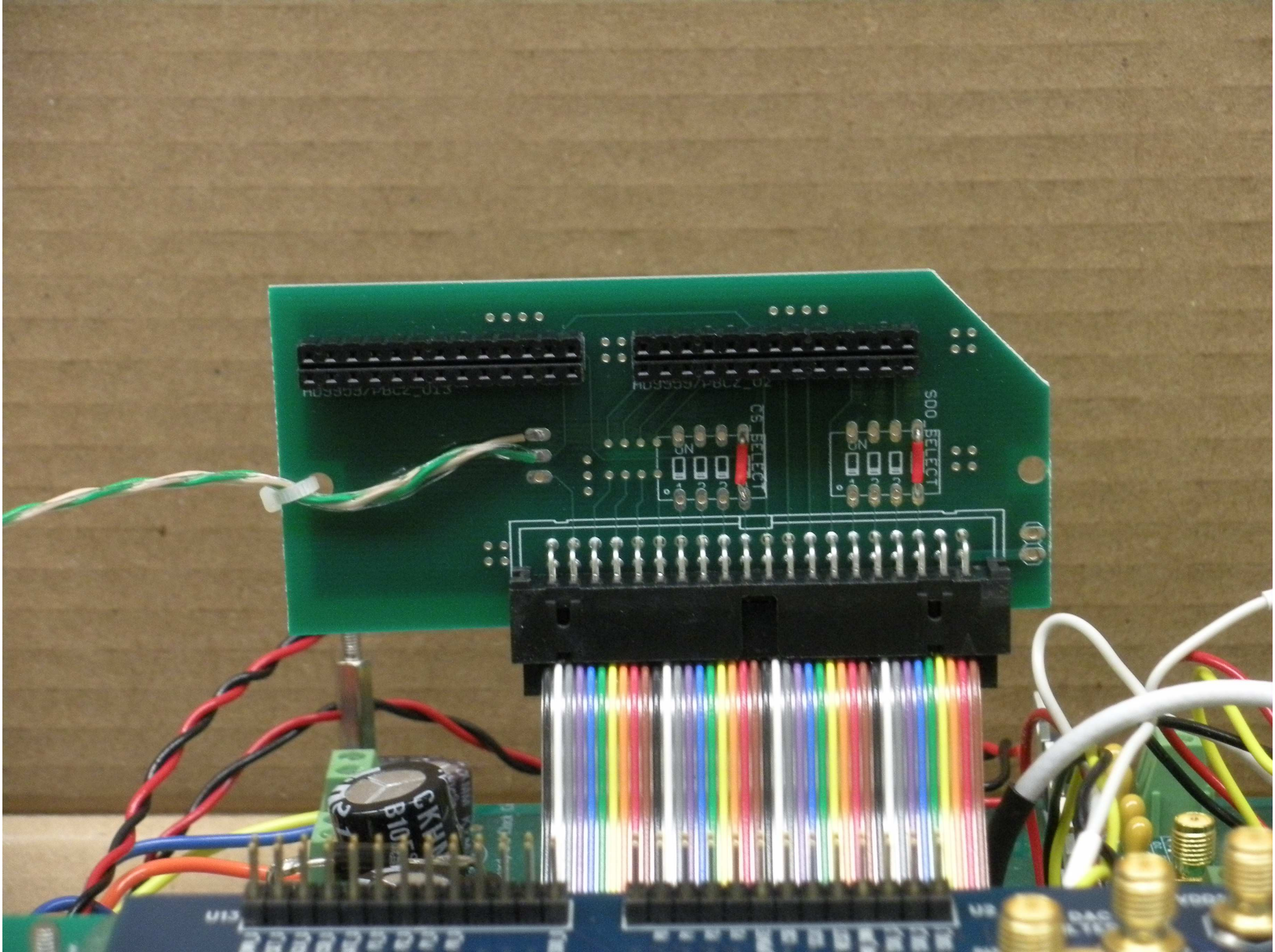
B.2. Microcontroller Board


Microcontroller Breakout Board
for DDS and ADC Control
rev. 2013-06-03
Christian Schneider

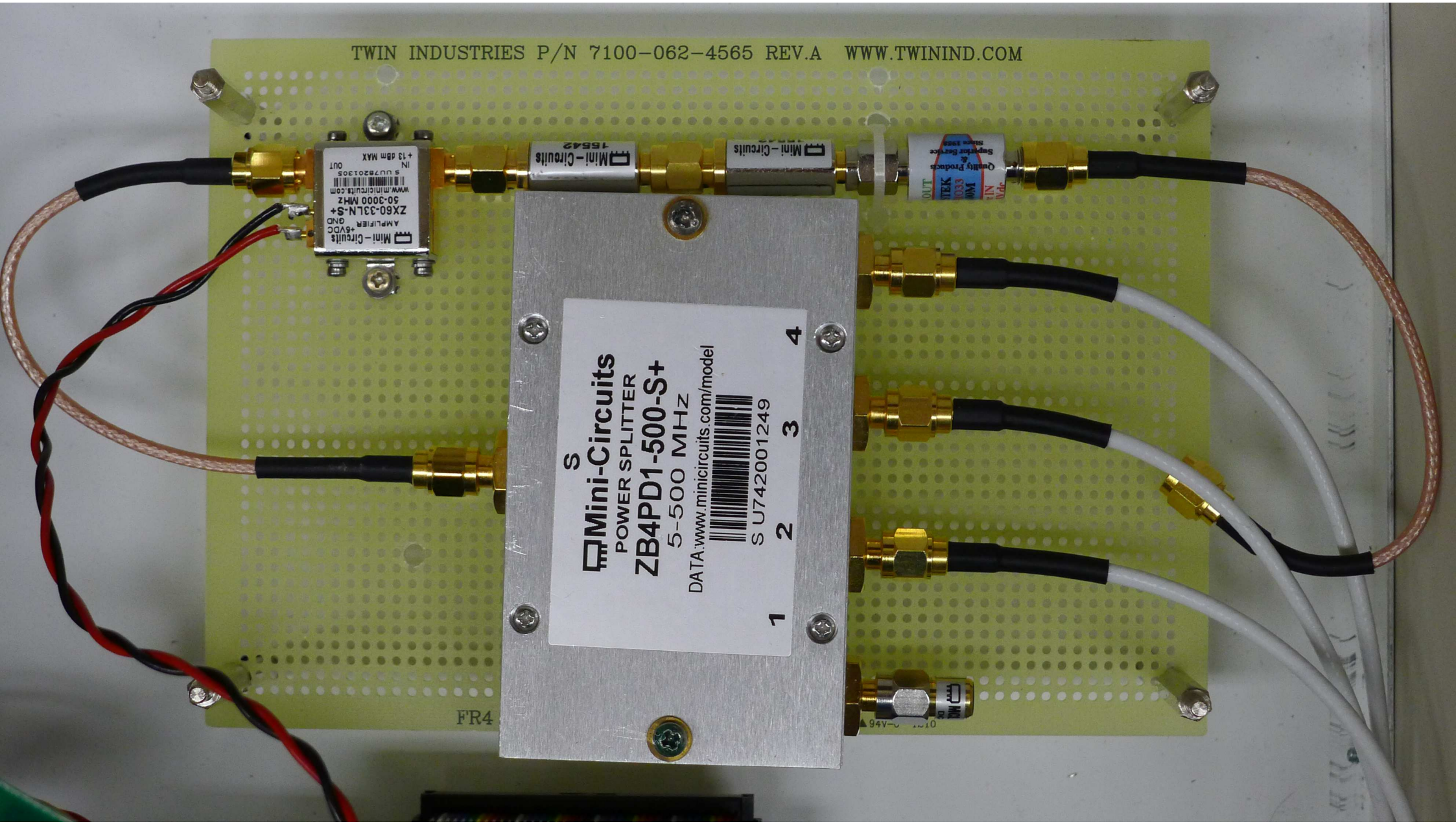

Microcontroller
for DDS and AD
rev. 2013-06-0
Christian Schne
Y11
X9
S1
LED3

B.3. DDS Chain Board


AD9959/PBCZ Chain Board
rev. 2013-06-06
AVDD1(1.8V)
DAC 1/59
FILTER OUT
J17
DAC 1/59
OUT
J5
J14
I/O UPDATE
IN
I/O UPDATE
OUT
R13
R12
R17
C43
C41
C40
C39
X1
C42
C25
C26
C30
U12
C61
PC_CTRL
PWR_DWN
RESET
SCLK
CSB
IO_UPDATE
P3
P2
P1
P0
SDIO
200 MHz LOW PASS FILTER
C36


CS SELECT
SDO SELECT
ON
ON

B.4. Clock Board


TWIN INDUSTRIES P/N 7100-062-4565 REV.A WWW.TWININD.COM
Mini-Circuits
POWER SPLITTER
ZB4PD1-500-S+
5-500 MHz
DATA:www.minicircuits.com/model
S U742001249
1 2 3 4
Mini-Circuits
AMPLIFIER
ZX60-33LN-S+
50-3000 MHz
+13 dBm MAX
IN OUT
Mini-Circuits
15542
Mini-Circuits
FR4

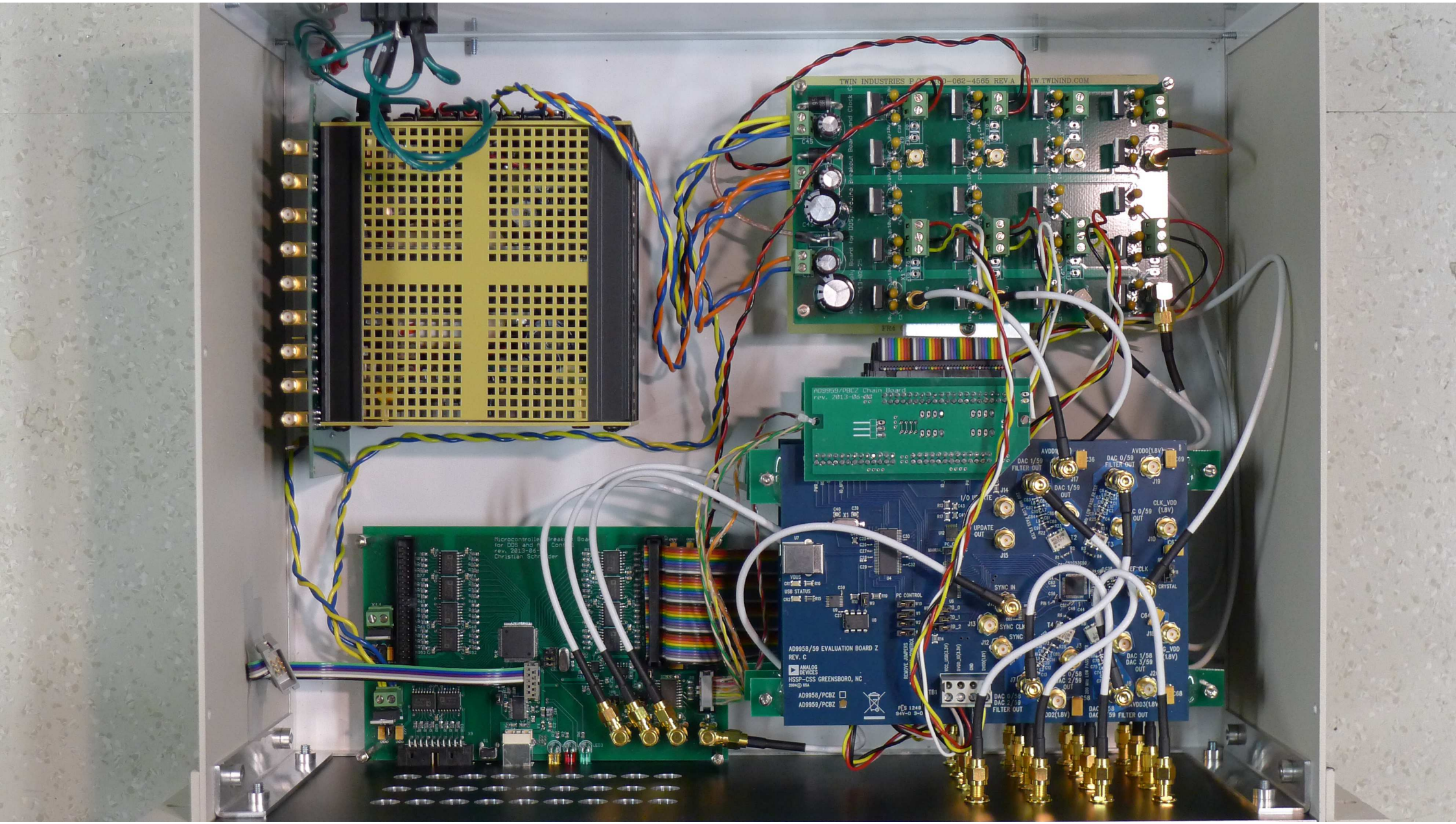
B.5. Zero-Crossing D-Type Flip-Flop

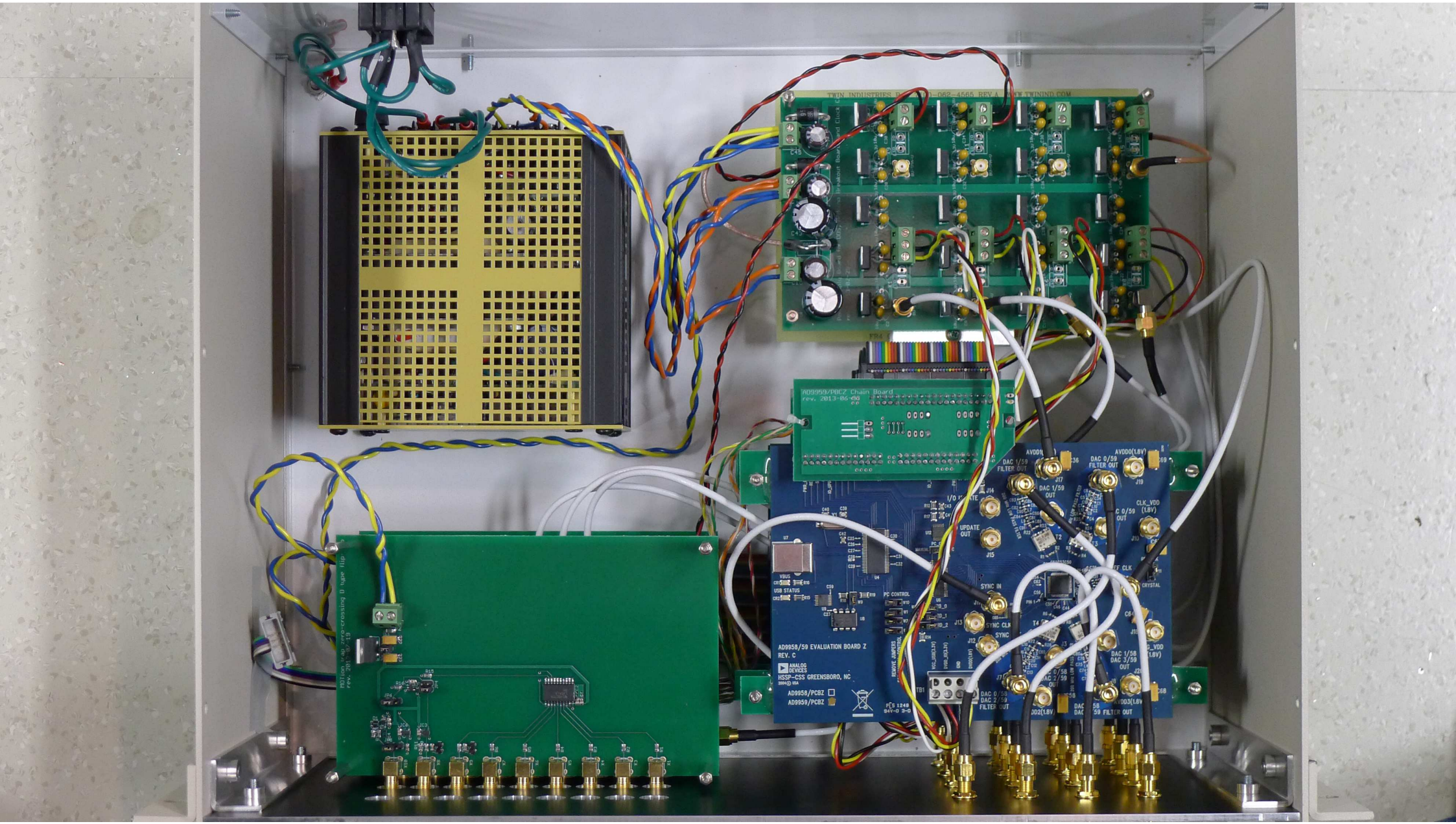
Motion trap zero-crossing D type flip-
rev. 2013-07-19
X1
X3
X4
X5
X6
X7
X9
X8
X10
R1
R2
R3
R4
R5
R6
R11
R15
R16
JP4
JP6
JP7
IC3
IC6
D1
C2
C5
U7
VBUS
USB STATUS
AD9958/59
REV. C
ANALOG DEVICES
HSSP-CSS
AD9958
AD9959

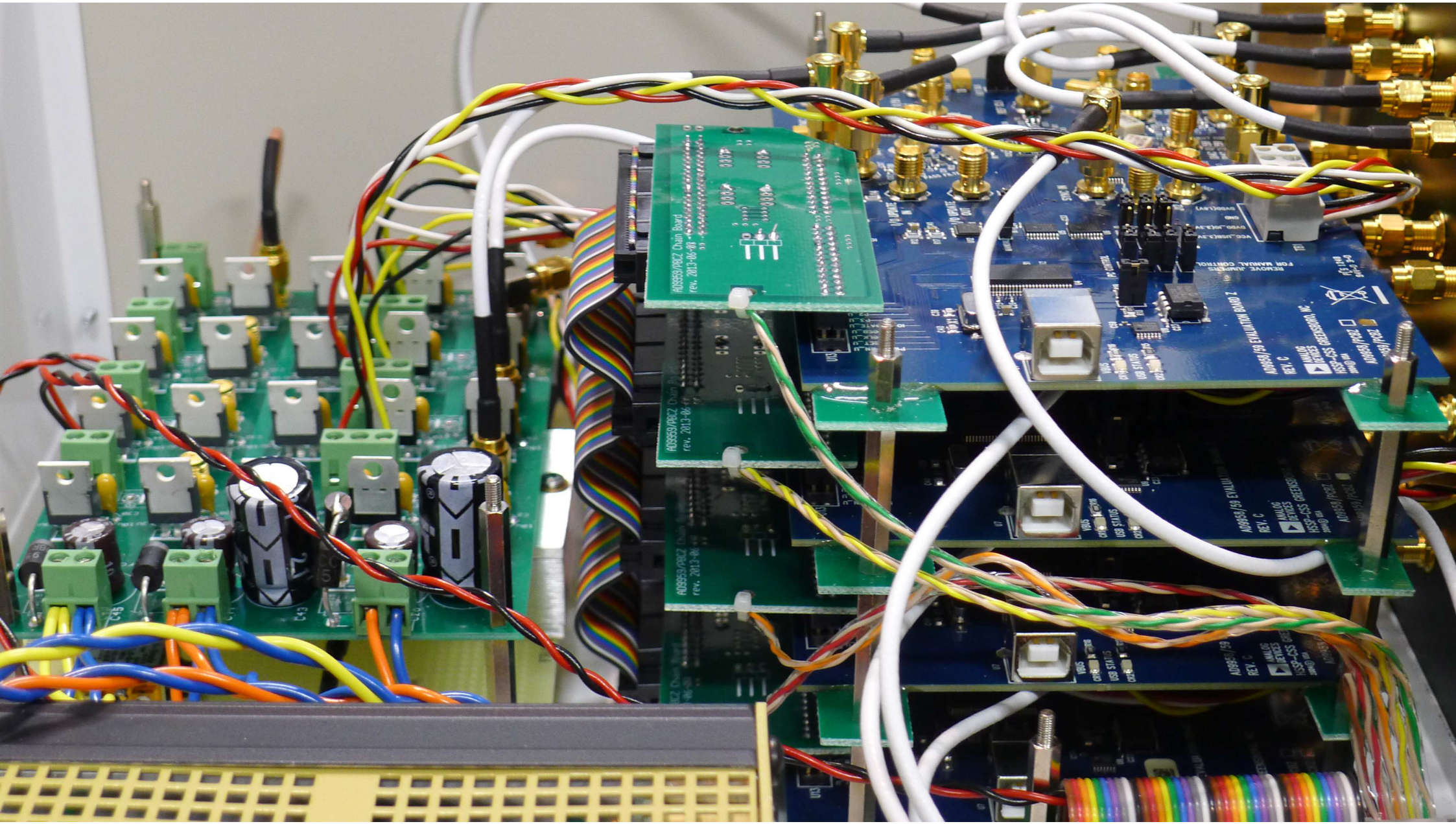
B.6. Power Supply Board

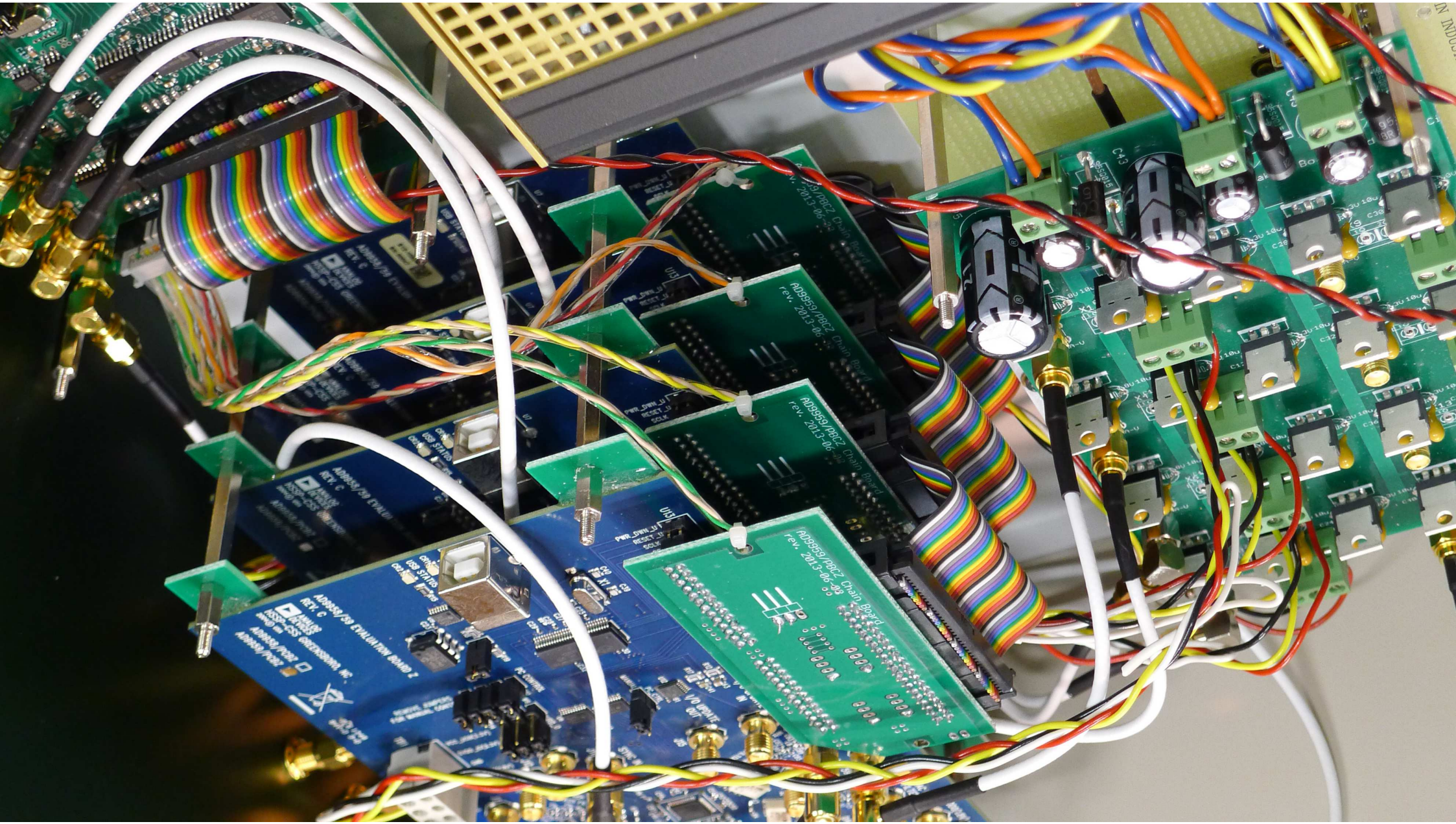
TWIN INDUSTRIES P/N 7100-062-4565 REV.A WWW.TWININD.COM
Power Supply Board for DDS, Arduino Breakout Board, and Clock Ci
rev. 2013-02-25

B.7. Complete Control Unit


AD9959/PCBZ Chain Board
rev. 2013-06-06
AD9958/59 EVALUATION BOARD Z
REV. C
ANALOG DEVICES
HSSP-CSS GREENSBORO, NC
AD9958/PCBZ
AD9959/PCBZ
USB STATUS
I/O UPDATE
UPDATE OUT
SYNC IN
SYNC CLK
SYNC
PC CONTROL
DAC 1/59 FILTER OUT
DAC 1/59 OUT
DAC 0/59 FILTER OUT
DAC 0/59 OUT
CLK_VDD (1.8V)
CRYSTAL
DAC 1/58 DAC 3/59 OUT
DAC 0/58 DAC 2/59 FILTER OUT
AVDDO(1.8V)
AVDDO3(1.8V)


AD9959/PCBZ Chain Board
rev. 2013-06-00
AD9958/59 EVALUATION BOARD Z
REV. C
ANALOG DEVICES
HSSP-CSS GREENSBORO, NC
AD9958/PCBZ
AD9959/PCBZ
DAC 1/59 FILTER OUT
DAC 1/59 OUT
DAC 0/59 FILTER OUT
AVDD0(1.8V)
UPDATE OUT
SYNC IN
SYNC CLK
SYNC
PC CONTROL
USB STATUS
CRYSTAL
CLK_VDD (1.8V)
DAC 1/58 DAC 3/59 OUT
DAC 0/58 DAC 2/59 OUT
DAC 0/59 DAC 2/59 FILTER OUT
AVDD3(1.8V)
REF CLK


AD9959/PBCZ Chain Board
rev. 2013-06-06
AD9959/59 EVALUATION BOARD Z
REV. C
ANALOG DEVICES
HSSP-CSS GREENSPRING, WC.
REMOVE JUMPERS FOR MANUAL CONTROL
USB STATUS
VBUS
C49


AD9959/PBC2 Chain Board
rev. 2013-06-29
AD9959/PBC2 Chain Board
rev. 2013-06-29
AD9959/PBC2 Chain Board
rev. 2013-06-29
AD9959/59 EVALUATION BOARD 2
ANALOG DEVICES
RSSK-CSS GREENSBORO, NC
AD9959/PCB2
AD9959/PCB2
USB STATUS
PC CONTROL
I/O UPDATE
PWR_DWN_U
RESET_U
SCLK
C43
C30
C32
C34
C10

B.8. Front Panel

UCLA | AMO
MOTion Control Unit
analog inputs
9 10 11 12 13 14 15 16 17
0 1 2 3 4 5 6 7 8
trigger
ref. in
out
controller
digital I/O
reset
USB
RX TX uC
DDS outputs
12 13 14 15
8 9 10 11
4 5 6 7
0 1 2 3

UCLA | AMO
MOTion Control Unit
analog inputs
9 10 11 12 13 14 15 16 17
0 1 2 3 4 5 6 7 8
trigger
ref. in out
controller
digital I/O reset USB RX TX uC
DDS outputs
12 13 14 15
8 9 10 11
4 5 6 7
0 1 2 3